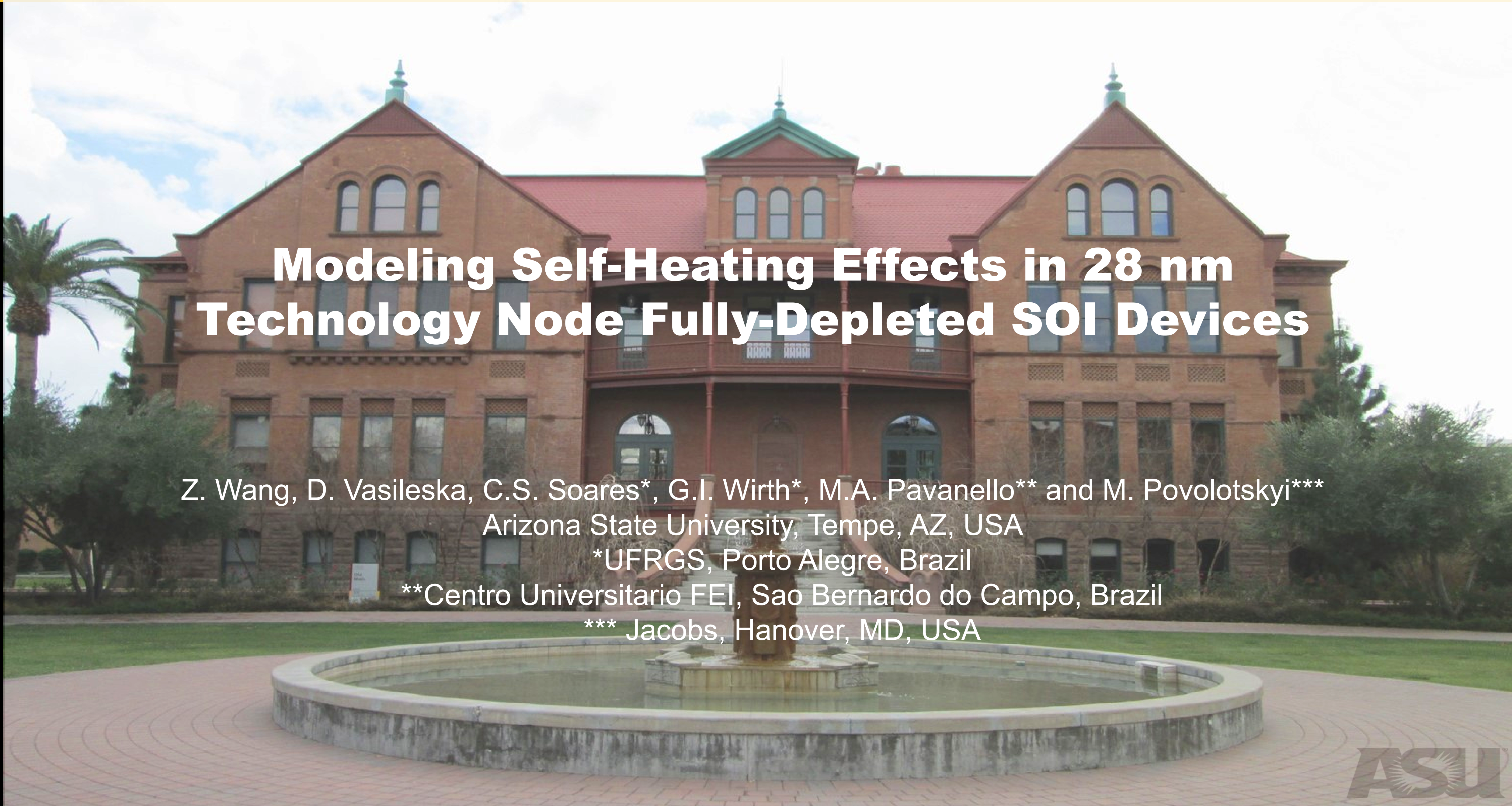

Modeling Self-Heating Effects in 28 nm Technology Node Fully-Depleted SOI Devices

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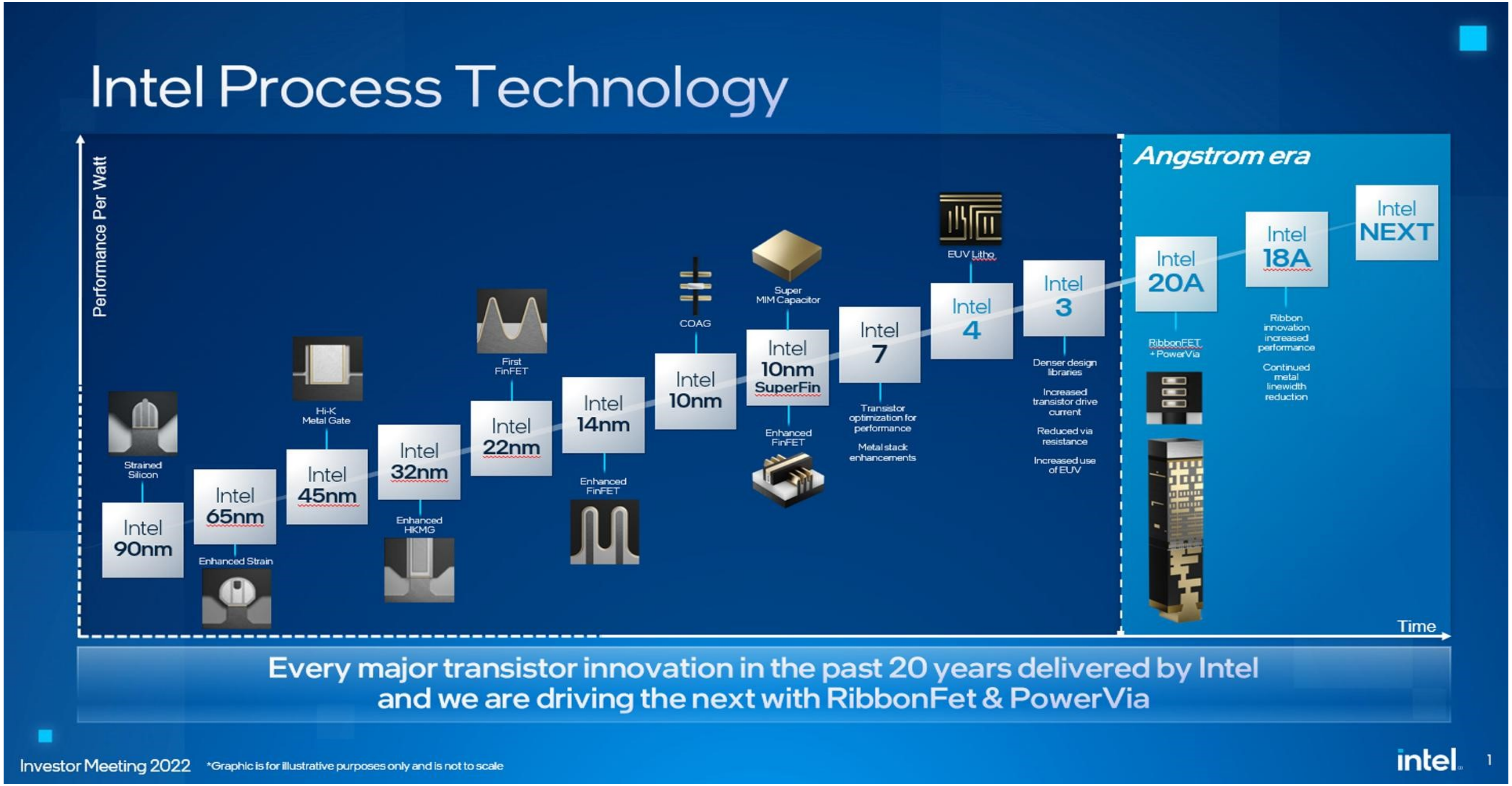
Talk Outline

- Technology Trends
- Challenges to TCAD: Multiscale Nature of Self-Heating
- Approaches to Modeling Self-Heating
- ASU Approach in More Details
- Modeling Self-Heating: Thermal Conductivity
- 28 nm Technology Node FD SOI Device
- Importance of Self-Heating
- Conclusions

Technology Trends:



Intel Process Technology

Performance Per Watt

Time

- Intel 90nm – Strained Silicon
- Intel 65nm – Enhanced Strain
- Intel 45nm – Hi-K Metal Gate
- Intel 32nm – Enhanced HKMG
- Intel 22nm – First FinFET
- Intel 14nm – Enhanced FinFET
- Intel 10nm – COAG
- Intel 10nm SuperFin – Super MIM Capacitor; Enhanced FinFET
- Intel 7 – Transistor optimization for performance; Metal stack enhancements
- Intel 4 – EUV Litho
- Intel 3 – Denser design libraries; Increased transistor drive current; Reduced via resistance; Increased use of EUV

Angstrom era

- Intel 20A – RibbonFET + PowerVia
- Intel 18A – Ribbon innovation increased performance; Continued metal linewidth reduction
- Intel NEXT

Every major transistor innovation in the past 20 years delivered by Intel and we are driving the next with RibbonFet & PowerVia

Investor Meeting 2022 *Graphic is for illustrative purposes only and is not to scale

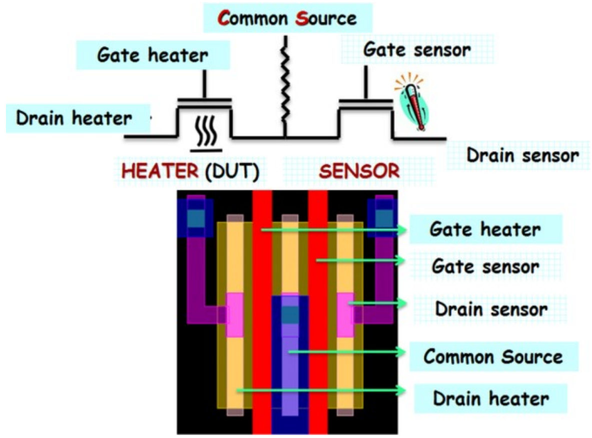
intel.

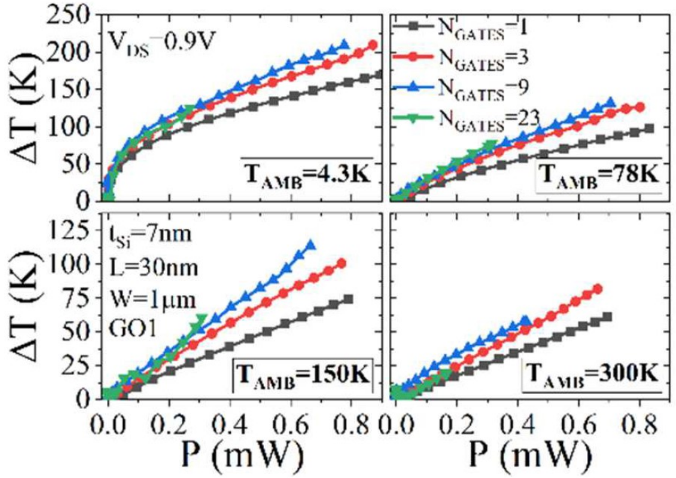
Effects:

- Random Dopant/Unintentional Dopant Fluctuations
- **Self-Heating**

Experimental Characterization:

- Heater-Sensor Approach [1]
- Gate Resistance Thermometry [2,3]





- Quantization of Charge, Tunneling and Quantum Interference

[1] E. Bury, B. Kaczer, P. J. Roussel, R. Ritzenthaler, K. Raleva, D. Vasileska, G. Groeseneken, "Experimental validation of self-heating simulations and projections for transistors in deeply scaled nodes", in Proceedings of IEEE, Reliability Physics Symposium, 2014 IEEE International, pp. XT. 8.1-XT. 8.6

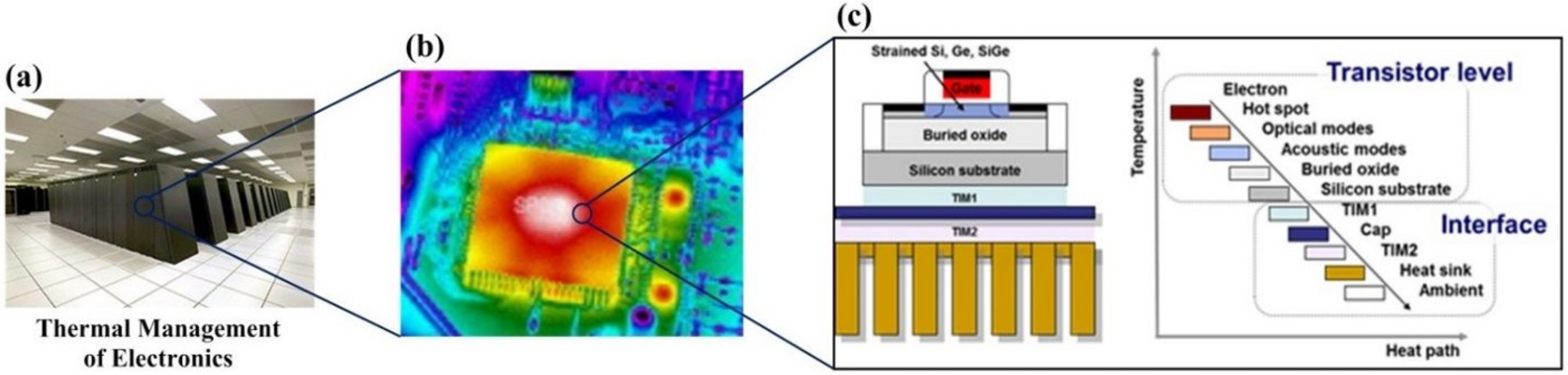
[2] K. Triantopoulos et al., "Self-heating effect in FDSOI transistors down to cryogenic operation at 4.2K", IEEE Trans. Electron Devices 66, no. 8, pp. 3498-3505 (2019).

[3] M. Casse et al., "FDSOI for cryoCMOS electronics: device characterization towards compact model", IEDM (2022)

Challenge to TCAD:

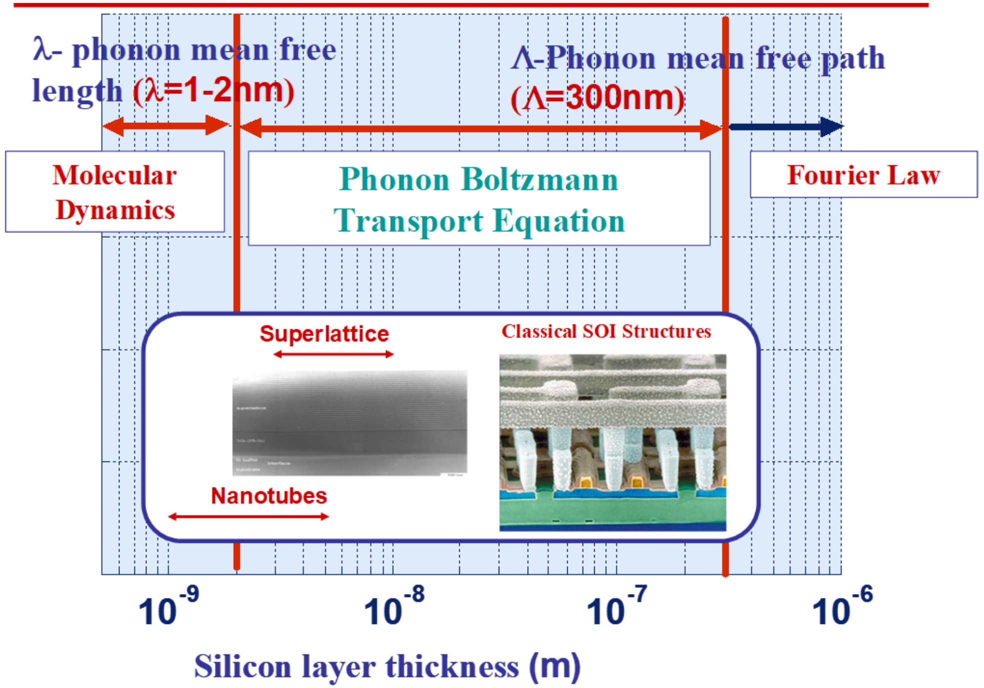
Multiscale Nature of Self-Heating

- Phonon-mediated thermal transport is inherently **multi-scale**:
  - The ***wave-length of phonons*** (considering phonons as waves) *is typically at the nanometer scale*;
  - *The **typical size of a phonon wave energy packet** is tens of nanometers*, while
  - *The **phonon mean free path** (MFP) can be as long as microns*.
- **Multi-scale thermal transport [1]:**
  - Different heat transfer physics across **different length scales**, and
  - The physics crossing different scales is interdependent and coupled.



[1] ***Phys.Chem.Chem.Phys.***, 2021, 23, 1785

Approaches to Modeling Self-Heating

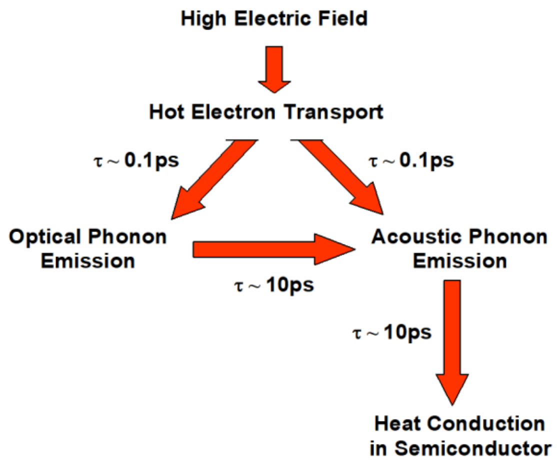


$$\left(\frac{\partial}{\partial t}+v_e(\mathrm{k})\cdot\nabla_r+\frac{e}{\hbar}E(\mathrm{r})\cdot\nabla_k\right)f=\sum_{\mathrm{q}}\left\{W_{e,\mathrm{q}}^{\mathrm{k+q}\to\mathrm{k}}+W_{a,-\mathrm{q}}^{\mathrm{k+q}\to\mathrm{k}}-W_{e,-\mathrm{q}}^{\mathrm{k}\to\mathrm{k+q}}-W_{a,\mathrm{q}}^{\mathrm{k}\to\mathrm{k+q}}\right\}$$

$$\left(\frac{\partial}{\partial t}+v_p(q)\cdot\nabla_r\right)g=\sum_{\mathrm{k}}\left\{W_{e,\mathrm{q}}^{\mathrm{k+q}\to\mathrm{k}}-W_{a,\mathrm{q}}^{\mathrm{k}\to\mathrm{k+q}}\right\}+\left(\frac{\partial g}{\partial t}\right)_{p-p}$$

ASU Approach:

Energy Balance Model [1,2]


High Electric Field

Hot Electron Transport

τ ~ 0.1ps

τ ~ 0.1ps

Optical Phonon Emission

Acoustic Phonon Emission

τ ~ 10ps

τ ~ 10ps

Heat Conduction in Semiconductor

$$C_{LO}\frac{\partial T_{LO}}{\partial t}=\frac{3nk_B}{2}\left(\frac{T_e-T_L}{\tau_{e-LO}}\right)+\frac{nm^*v_d^2}{2\tau_{e-LO}}-C_{LO}\left(\frac{T_{LO}-T_A}{\tau_{LO-A}}\right),$$

$$C_A\frac{\partial T_A}{\partial t}=\nabla\cdot(\underset{\uparrow}{k_A}\nabla T_A)+C_{LO}\left(\frac{T_{LO}-T_A}{\tau_{LO-A}}\right)+\frac{3nk_B}{2}\left(\frac{T_e-T_L}{\tau_{e-L}}\right).$$

[1] J. Lai and A. Majumdar, “Concurrent thermal and electrical modeling of submicrometer silicon devices”, J. Appl. Phys., Vol. 79, 7353 (1996).

[2] K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov,”Modeling Thermal Effects in Nanodevices”, IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008.

Approaches to Modeling Self-Heating, Cont'd

Heat Conduction Equation:

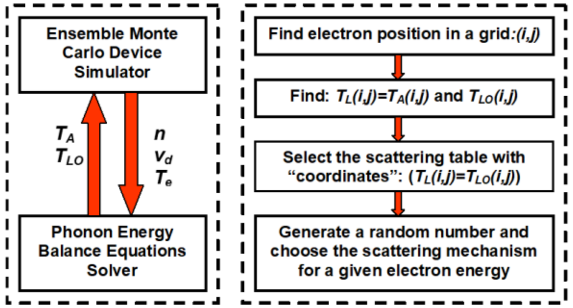
$$\boxed{C_\rho \frac{\partial T_L}{\partial t} = \nabla \cdot (\kappa \nabla T_L) + \dot{q}_V}$$

- $\dot{q}_V = \frac{1}{t}\frac{d}{dV}\sum(\hbar\omega_{em} - \hbar\omega_{ab})$ Net phonon emission approach [1,2]
- $\dot{q}_V = C_{Lo}\left(\frac{T_{Lo}-T_L}{\tau_{Lo-A}}\right) + \frac{3nk_B}{2}\left(\frac{T_e-T_L}{\tau_{e-L}}\right) + \frac{nm^* {v_d}^2}{2\tau_{e-L}}$ Lai and Majumdar [3]
- $\dot{q}_V = \vec{J} \cdot \vec{E}$+ corrections Wachutka model [4]

[1] N. J. Pilgrim, "Electro-thermal Monte Carlo simulation of semiconductor devices", PhD Dissertation, University of Leeds, UK, 2003.
[2] E. Pop, R. W. Dutton, K. E. Goodson, "Analytic band Monte Carlo model for electron transport in Si including acoustic and optical phonon dispersion", J. Appl. Phys., Vol. 96, 4998 (2004).
[3] J. Lai and A. Majumdar, "Concurrent thermal and electrical modeling of submicrometer silicon devices", J. Appl. Phys. , Vol. 79, 7353 (1996).
[4] Wachutka, G.K., "Rigorous Thermodynamic Treatment of Heat Generation in Semiconductor Device Modeling", *IEEE Trans., Computer-Aided Design* Vol. 9, No. 11 (1990): 1141-1149.

ASU Approach in More Details

Exchange of variables in the electro-thermal solver



Ensemble Monte Carlo Device Simulator

T_A T_{LO}

n v_d T_e

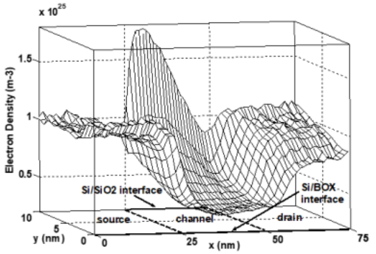
Phonon Energy Balance Equations Solver

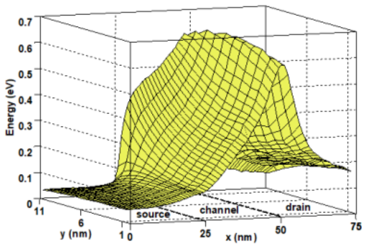
Find electron position in a grid:*(i,j)*

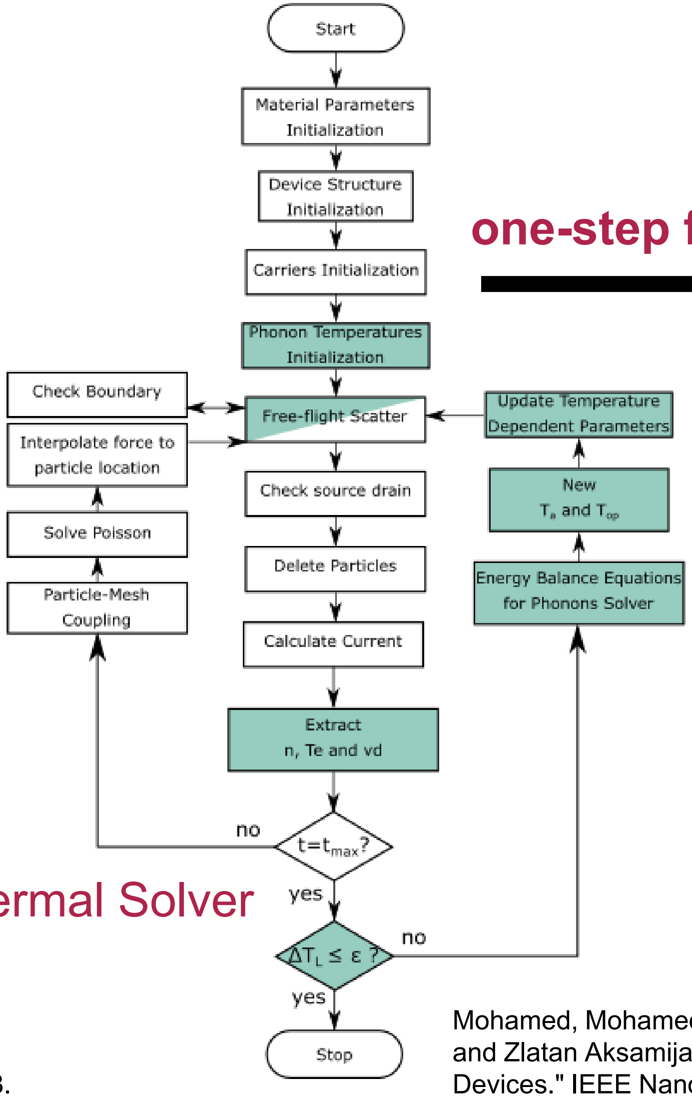
Find: $T_L(i,j)=T_A(i,j)$ and $T_{LO}(i,j)$

Select the scattering table with "coordinates": $(T_L(i,j)=T_{LO}(i,j))$

Generate a random number and choose the scattering mechanism for a given electron energy







Start

Material Parameters Initialization

Device Structure Initialization

Carriers Initialization

Phonon Temperatures Initialization

Check Boundary

Interpolate force to particle location

Solve Poisson

Particle-Mesh Coupling

Free-flight Scatter

Check source drain

Delete Particles

Calculate Current

Extract n, Te and vd

$t=t_{max}$?

no

yes

$\Delta T_L \le \varepsilon$?

no

yes

Stop

Update Temperature Dependent Parameters

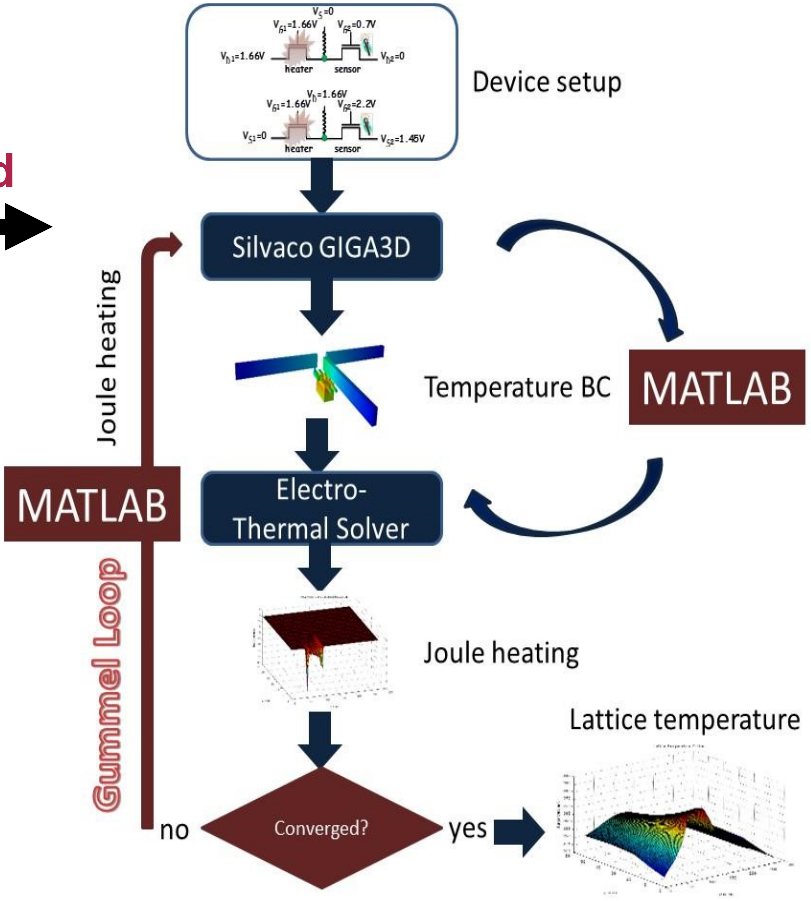
New T_a and T_{op}

Energy Balance Equations for Phonons Solver

Electro-Thermal Solver

one-step forward

Multi-Scale Electro-Thermal Solver



Device setup

Silvaco GIGA3D

Temperature BC

MATLAB

Joule heating

Electro-Thermal Solver

MATLAB

Gummel Loop

Joule heating

Lattice temperature

no

Converged?

yes

K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, "Modeling Thermal Effects in Nanodevices", IEEE Transactions on Electron Devices, vol. 55, issue 6, pp. 1306-1316, June 2008.

Mohamed, Mohamed, Katerina Raleva, Umberto Ravaioli, Dragica Vasileska, and Zlatan Aksamija. "Phonon Dissipation in Nanostructured Semiconductor Devices." IEEE Nanotechnology Magazine (2019): 1. Web.

Modeling Self-Heating:

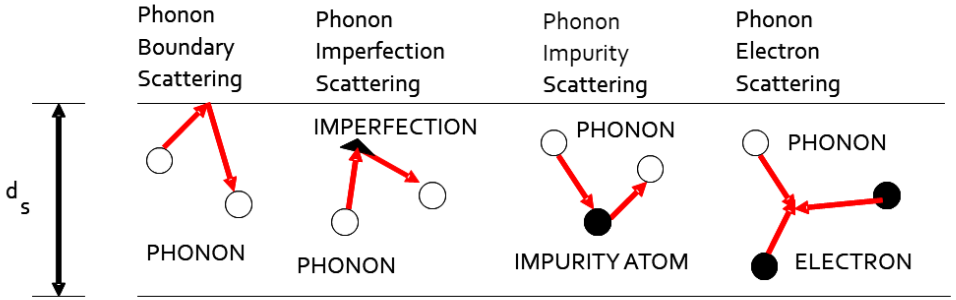
Thermal Conductivity

A measure of a material's ability to transfer thermal energy by conduction.

Thermal conductivity *k* has two different contributions: $\boldsymbol{\kappa = \kappa_{phonon} + \kappa_{electron}}$

- The electronic contribution to the thermal conductivity can be calculated using the Wiedemann-Franz law.
- The phonon contribution depends upon:
  - Scattering by Lattice Imperfections
  - Defects, dislocations, ***boundaries***

    (ELASTIC, energy and momentum are conserved)
  - Phonon-Electron Scattering
  - **Phonon-Phonon Interactions**
    - NORMAL N – processes → Energy and momentum are conserved
    - UMKLAPP U-processes → Only energy is conserved

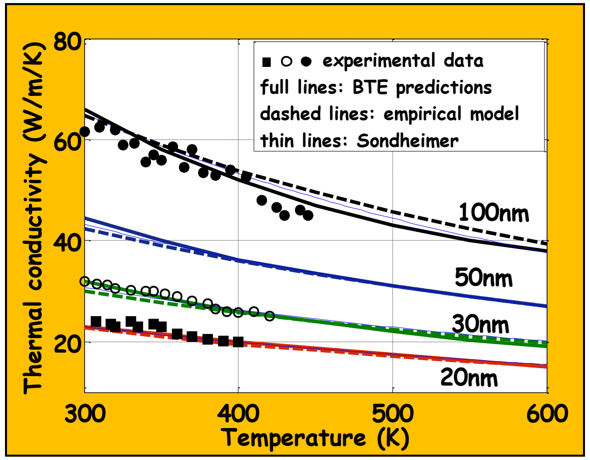


Phonon-Boundary Scattering (thin films)

$$\kappa(z)=\kappa_0(T)\int_0^{\pi/2}\sin^3\theta\left\{1-\exp\left(-\frac{a}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{a-2z}{2\lambda(T)\cos\theta}\right)\right\}d\theta$$

$$\lambda(T)=\lambda_0(300/T)$$

$$\kappa_0(T)=\frac{135}{a+bT+cT^2}\quad \mathrm{W/m/K}$$



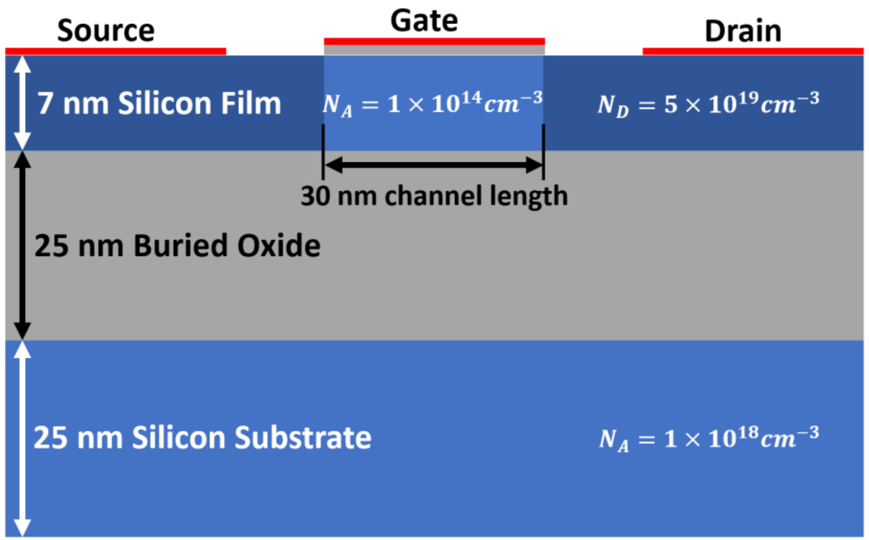
Experimental Data:
M. Asheghi,., M. N. Touzelbaev., K. E. Goodson, Y. K. Leung, and S. S. Wong., ASME Journal of Heat Transfer, Vol.120, pp. 30-33, 1998.

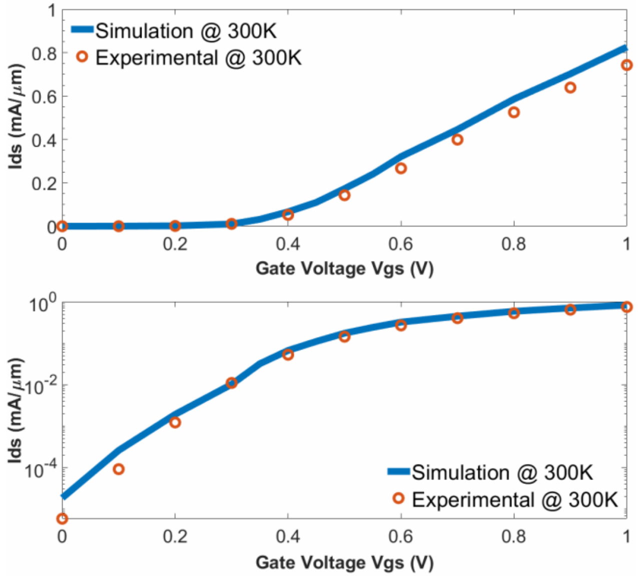
D. Vasileska, K. Raleva and S. M. Goodnick, "Electrothermal Studies of FD SOI Devices That Utilize a New Theoretical Model for the Temperature and Thickness Dependence of the Thermal Conductivity", IEEE Transactions on Electron Devices, Vol. 57, pp. 726 – 728 (2010).

28 nm Technology Node FD SOI Device

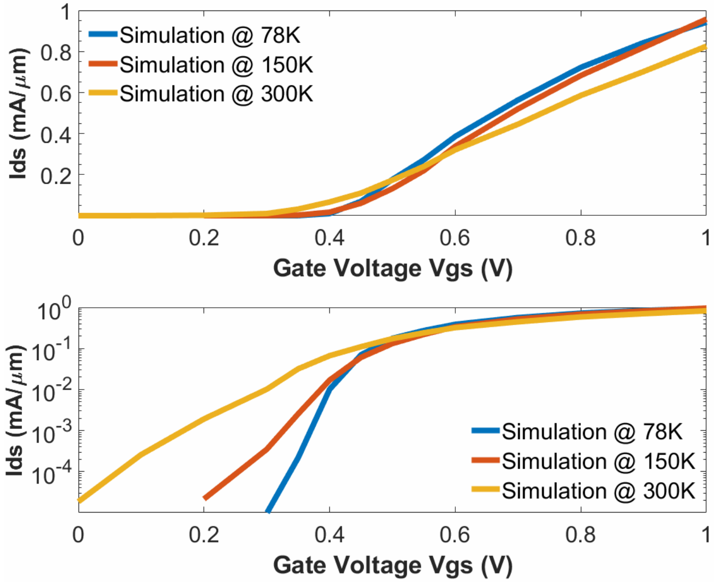
Quantum Features:

- Superposition of states ➔ Phase coherence ➔ Low-temperature ➔ No scattering
- Entanglement
- Quantum Tunneling





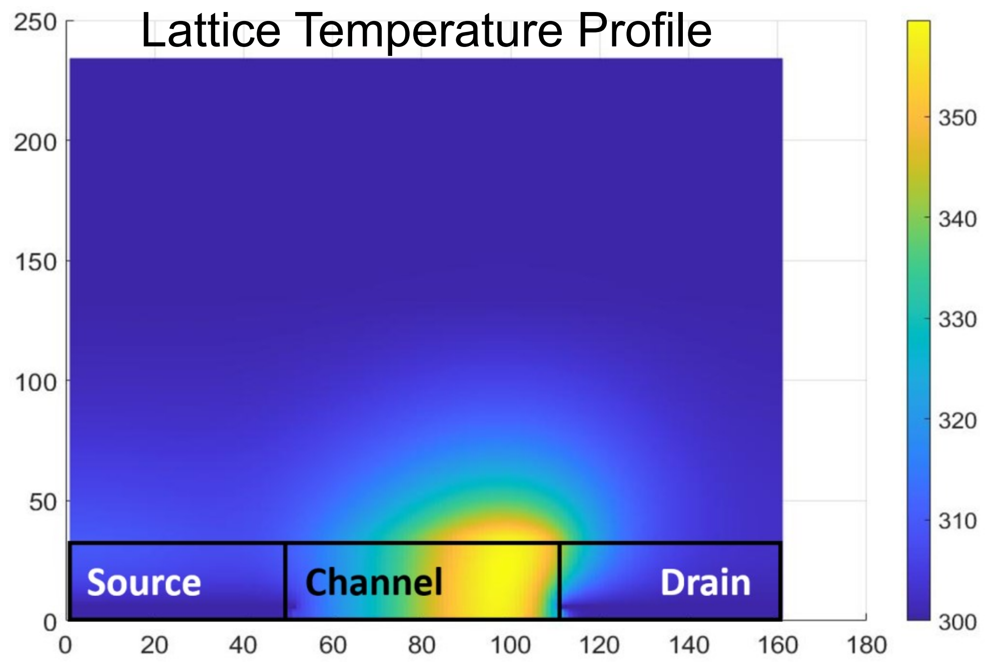
Simulated transfer characteristics compared with available experimental data from Ref. [1] at T=300K. The applied drain voltage is Vds=0.9V.



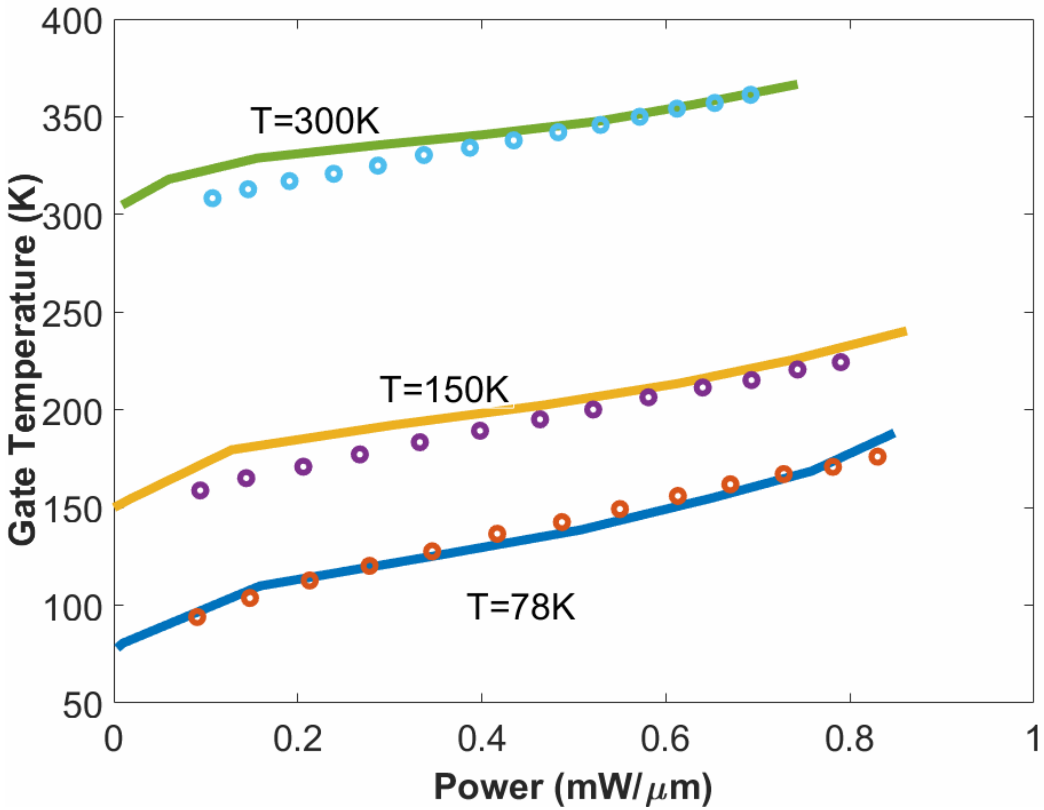
Simulated transfer characteristics at 78K, 150K and 300K. The applied drain voltage is Vds=0.9V.

[1] M. Casse et al., “FDSOI for cryoCMOS electronics: device characterization towards compact model”, IEDM (2022)

Importance of Self-Heating



- Lattice temperature profile at ambient temperature T=300K for Vgs=0.6V and Vds=0.9V.
- We used the following boundary conditions in the simulation:
  - Fixed temperature T=300K at source and drain contacts,
  - Zero heat flux at the gate contact.



Comparison of simulated (solid lines) and experimental (open circles) temperature under the gate for various input powers at T=78K, 150K and 300K.

Conclusions

- A 2D/3D electro-thermal device simulator has been developed at ASU to study self-heating effects in:
    - FD SOI Devices, nanowire transistors, dual gate device structures, FinFETs, CMOS inverters and simple two transistor (CS and CD) circuits.
- Low temperature simulations of FD SOI devices confirm the experimental findings that self-heating is very important at cryogenic temperatures.

This work was supported in part by multiple grants from

NSF, ONR, ARL.

Special thanks to all my students and colleagues who contributed significantly to the work presented.

Thank You!