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Transport and Edge Passivation

A few results

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Silvaco Inc., Purdue U.

IWCN 2023

Nemo5 – nanohub.org

⇔ Nemo5Pro

⇔ VictoryAtomistic

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SILVACO Tools IP Solutions Services Support

Silvaco, Purdue Team Up to Bring Scalable Atomistic TCAD Solutions For Next Generation Semiconductor Devices And Materials

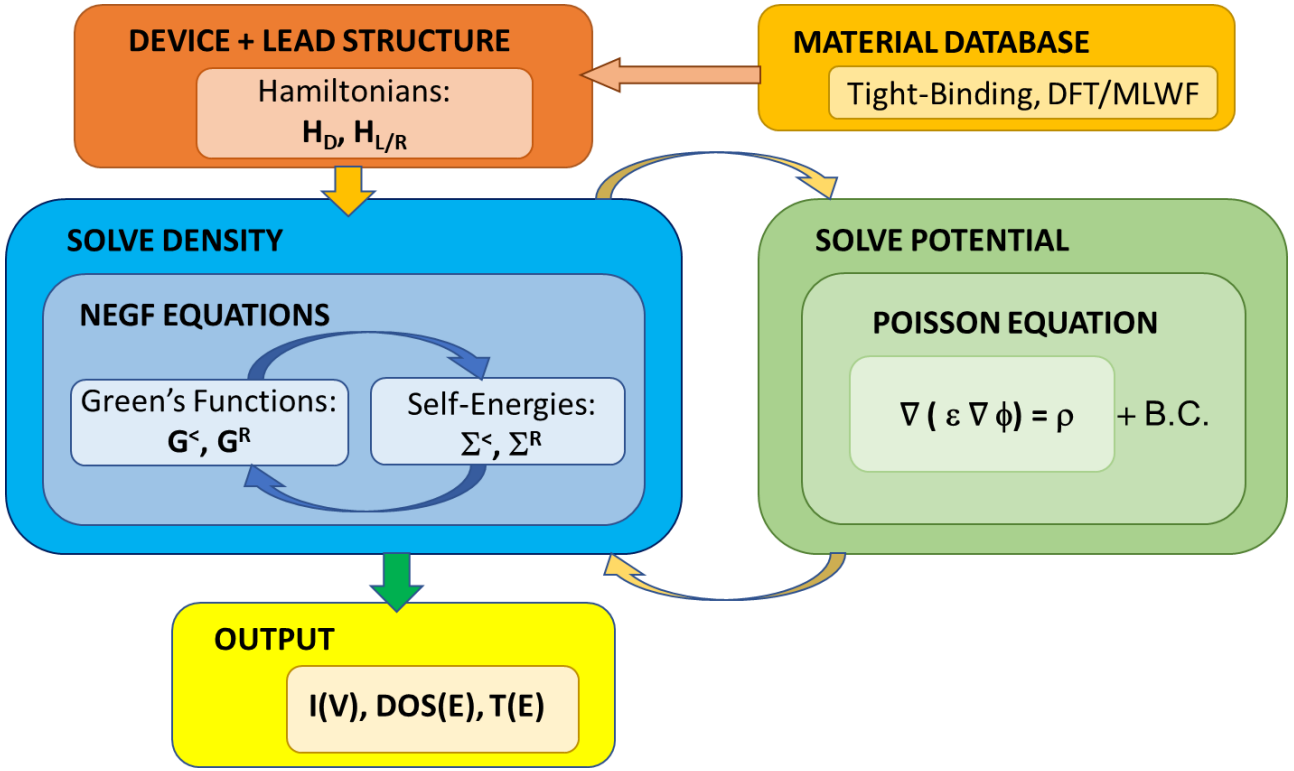
Santa Clara, California – West Lafayette, Ind. August 24, 2018 – Silvaco Inc., Purdue University and Purdue Research Foundation, announced Friday (Aug. 24) the formation of an innovative partnership aimed at extending Moore's law by modeling and simulating transistors and new memory technologies that approach atomistic scale in next generation semiconductor processes and materials.

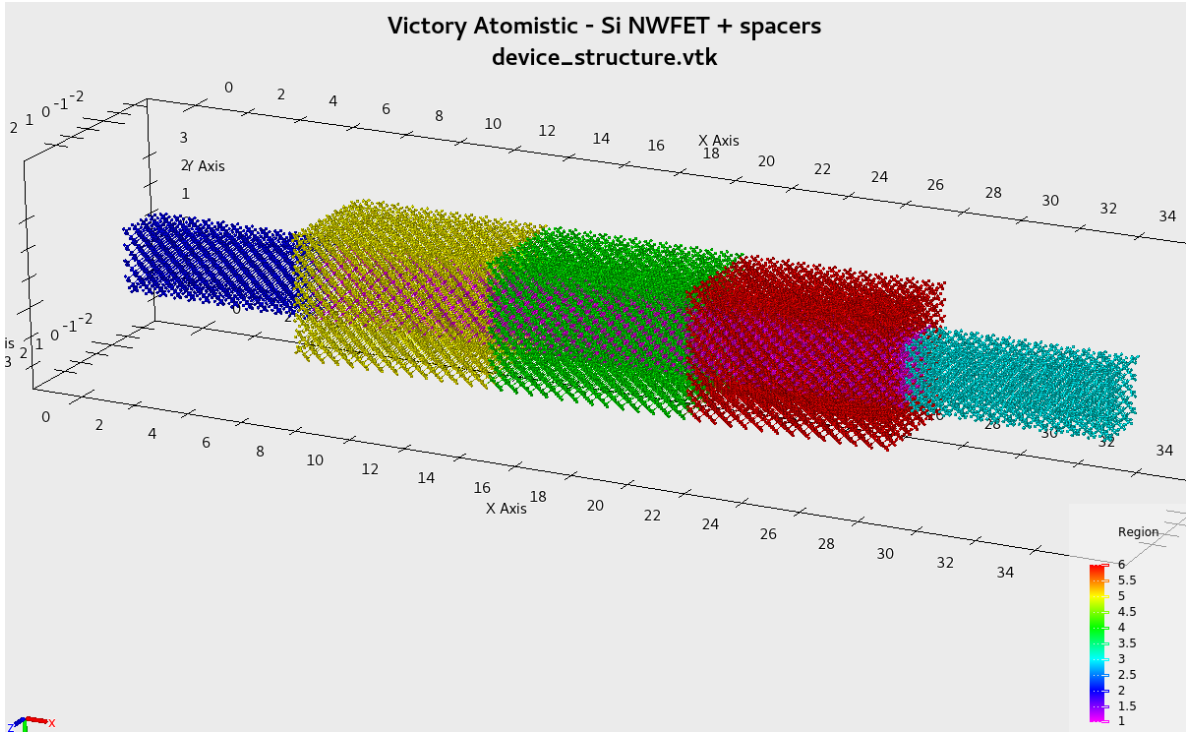
Silvaco will license Purdue University intellectual property from the Purdue Research Foundation, a private and nonprofit foundation created to advance the university's mission, sponsor research and open an office in the Purdue Technology Center.

Silvaco is a leader for more than 20 years in the TCAD market for semiconductor device and process simulation and its latest Victory™ TCAD tools are currently deployed in leading semiconductor companies worldwide. The agreement involves the commercialization of the NEMO tool suite, an atomistic nanoelectronics modeling and simulation tool that has been used by leading semiconductor companies as the golden device simulation tool for investigation of advanced physics phenomena aimed at extending Moore's law. The goal of this collaboration is to link NEMO with Silvaco's Virtual Wafer Fab™ to provide the market with a true ab-initio to circuit level integrated co-optimization design platform.

"We are very excited to bring together the strong research expertise of the Purdue team in atomistic simulation along with Silvaco's strong background in TCAD, modeling and circuit simulation," said Eric Guichard, vice president of the TCAD division at Silvaco. "The partnership will result in a powerful solution that enables path finding of advanced semiconductors well before running silicon which ultimately saves time-to-market and hundreds of millions of

Prototyping and Engineering

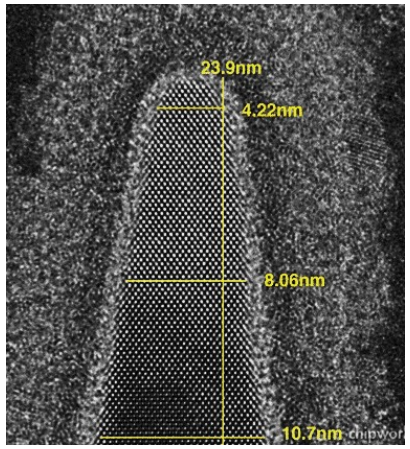




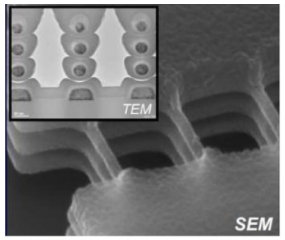
Vic-Atomistic renders atomic-scale TCAD easy keeping all the complexity inside

FinFET, **NS**heet-FET, **NW**ire-FET

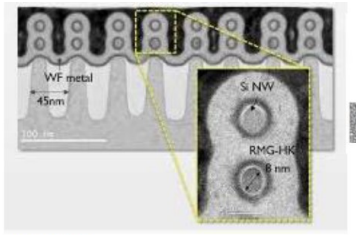
- FinFET: fin width ↘, fin height ↗ ⇔ smaller fin pitch



chipworksrealchips.blogspot.com/2012/04/intels-22-nm-trigate-transistors.html



LETI



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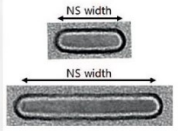
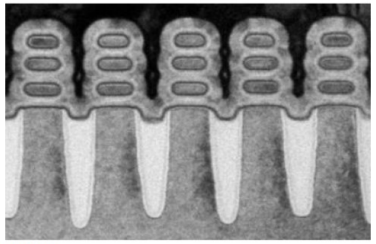
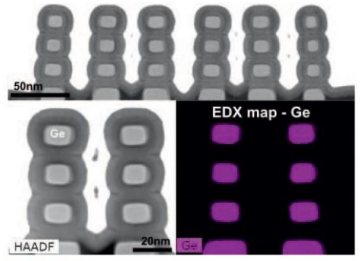


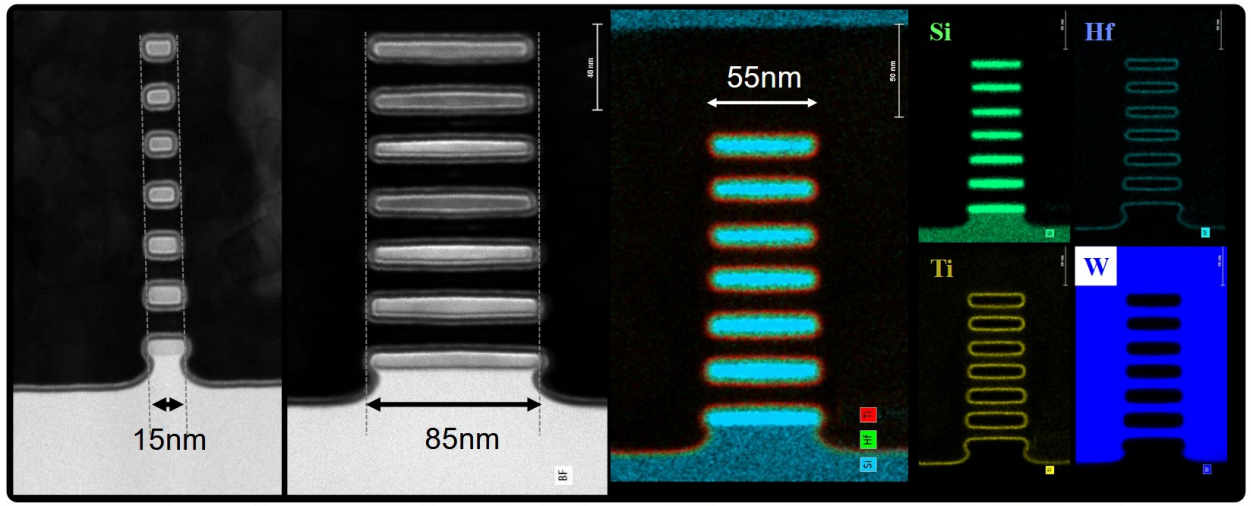
SAMSUNG



IBM



TSMC



GAA NS transistors with 7 stacked channels from tall and straight (SiGe/Si) fins.

S. Barraud (LETI) VLSI 2020

- **Low aspect ratio**, better **electrostatic control**
- T_{Si} ~ 5 – 7 nm, L_{CH} = 2x – 3x T_{Si}
- # stacked channels ↗, NS width ↗ ⇔ I_{sat} ↗, delay ↘

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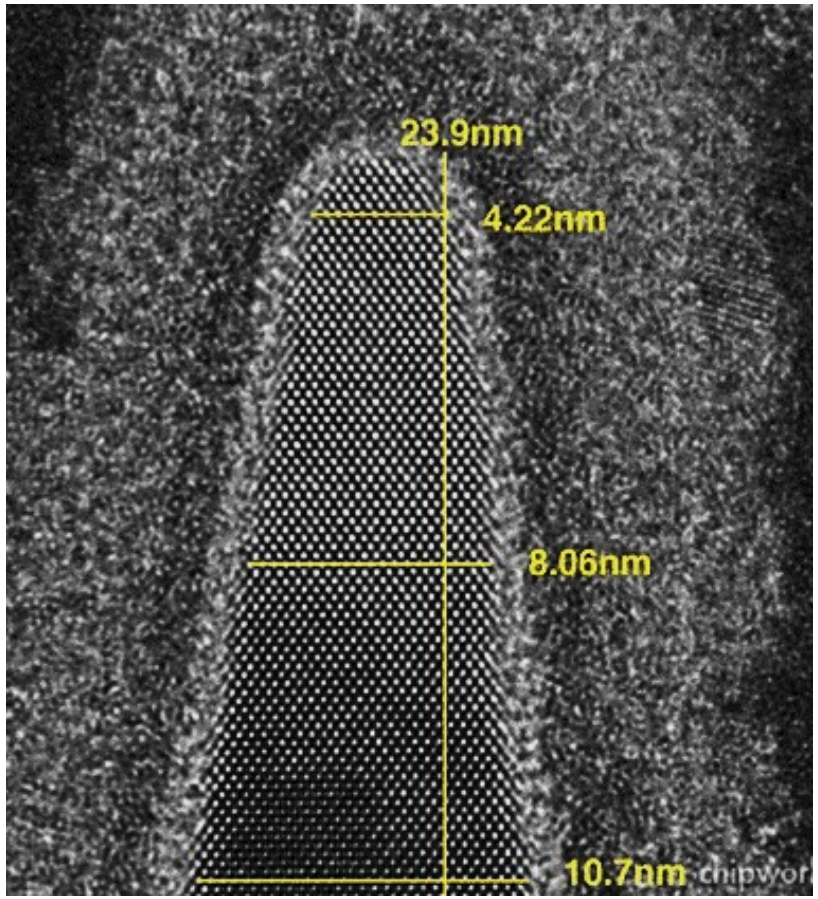
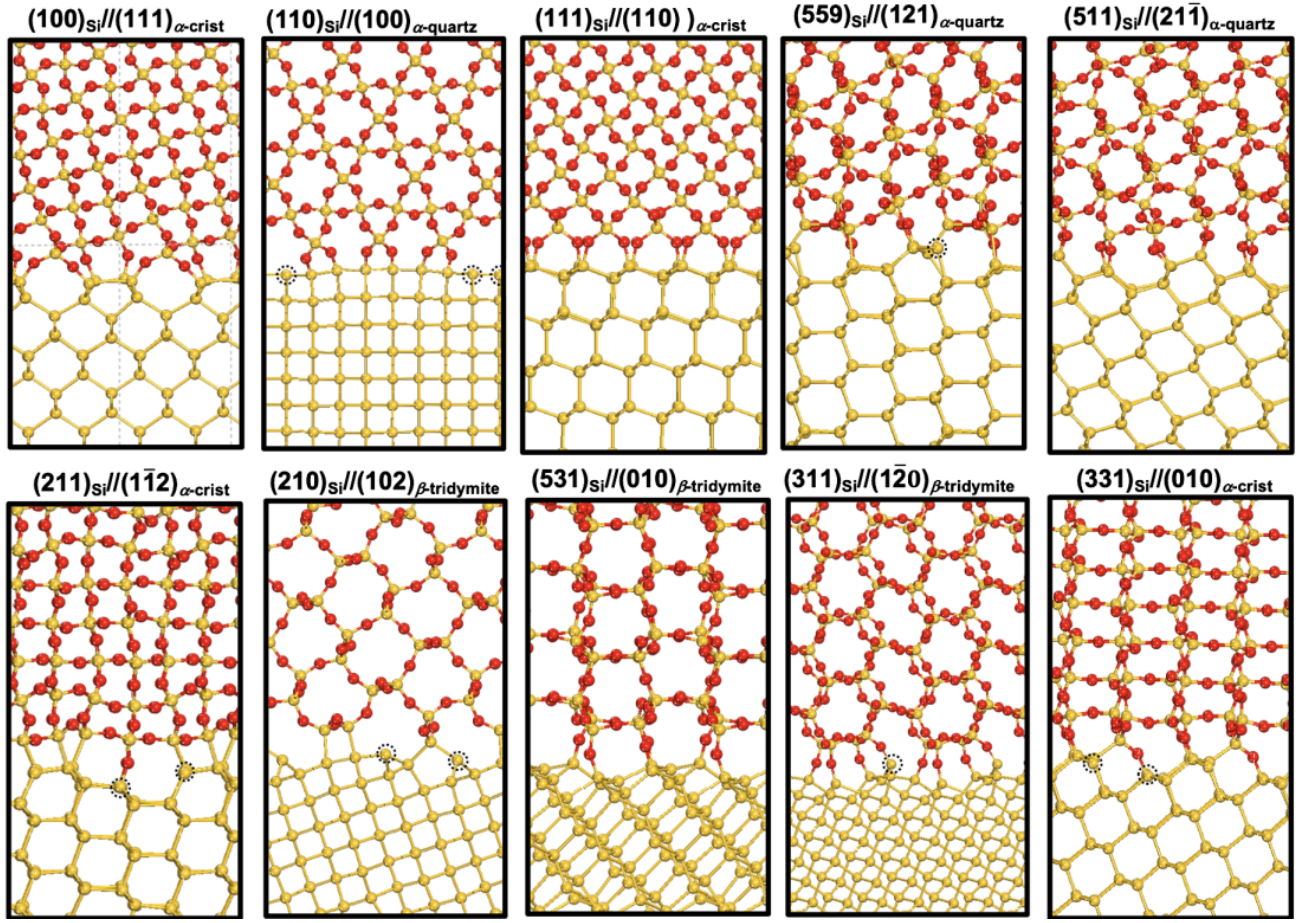
Silicon dioxide from silicon oxidation

- SiO_2 is very well-known: this is an amorphous structure

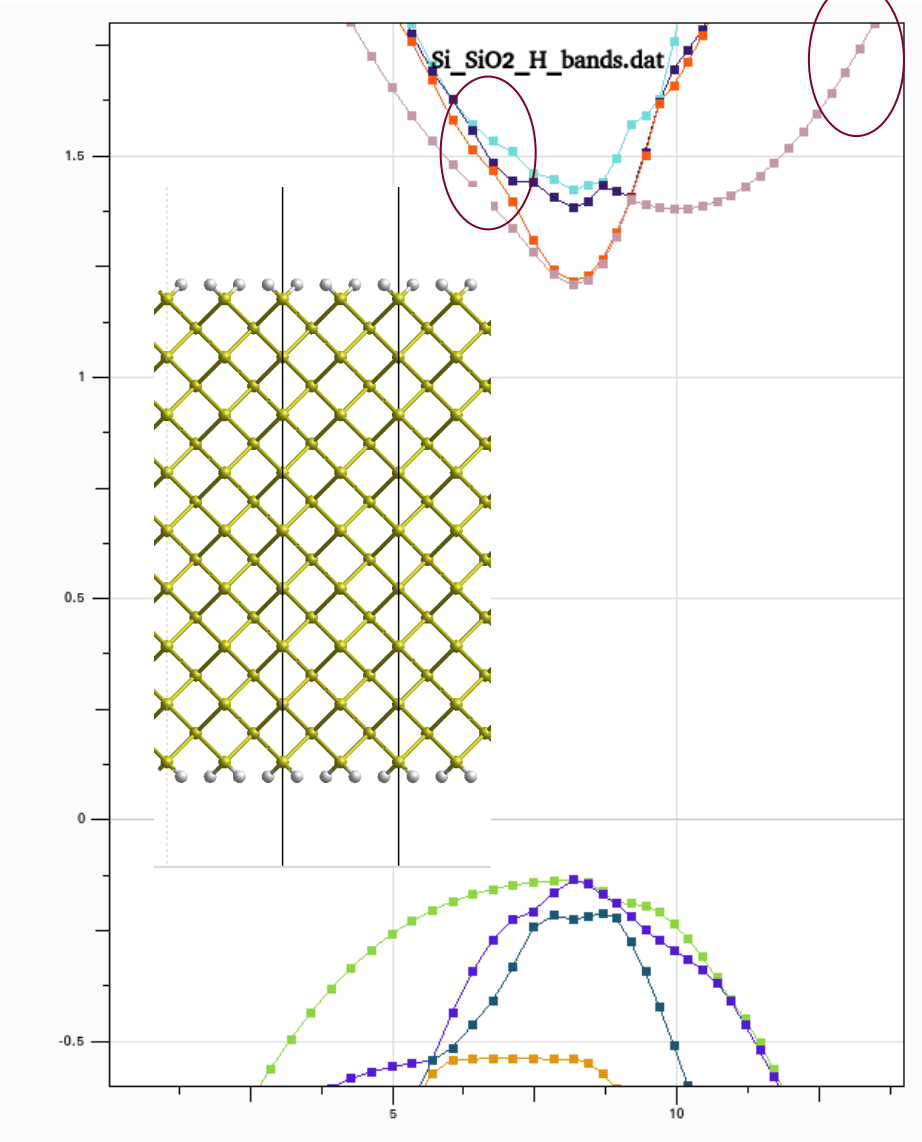


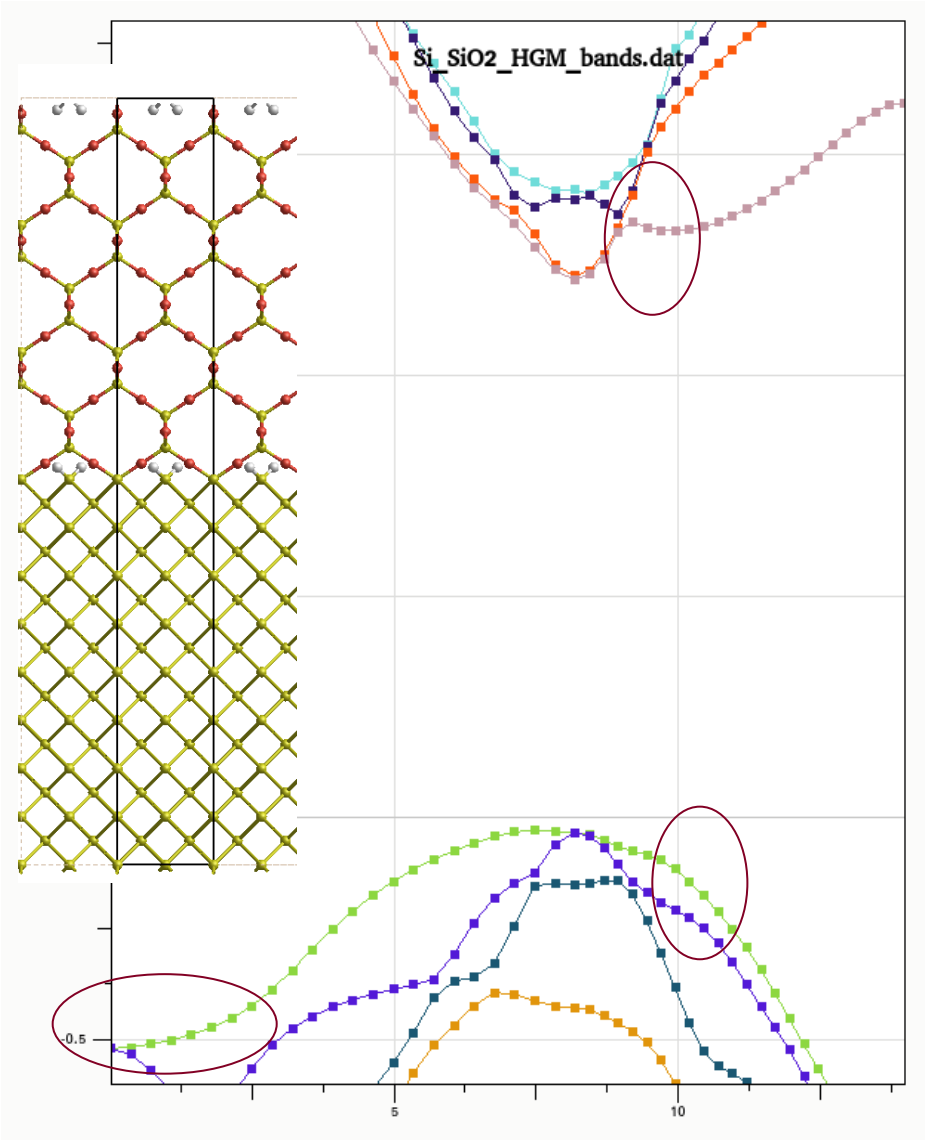
PHYSICAL REVIEW LETTERS **128,** 226102 (2022)



Si-termination: Impact on the Band Structure

- 2.17 nm thin layer of Si with H- and a mixture of H- and O- termination





- DFT/GGA simulation with rigid band gap correction (Siesta)
- H atoms are relaxed
- SiO_2 and Si atoms are kept fixed, constrained by c-Si

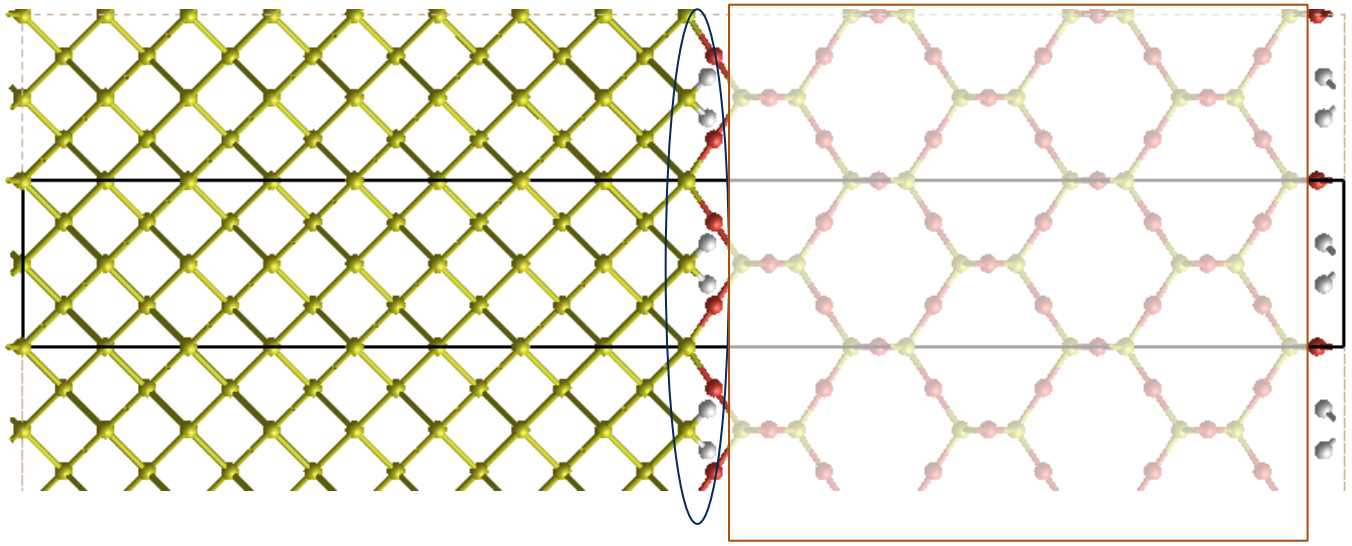
NEGF with an Implicit Passivation Scheme

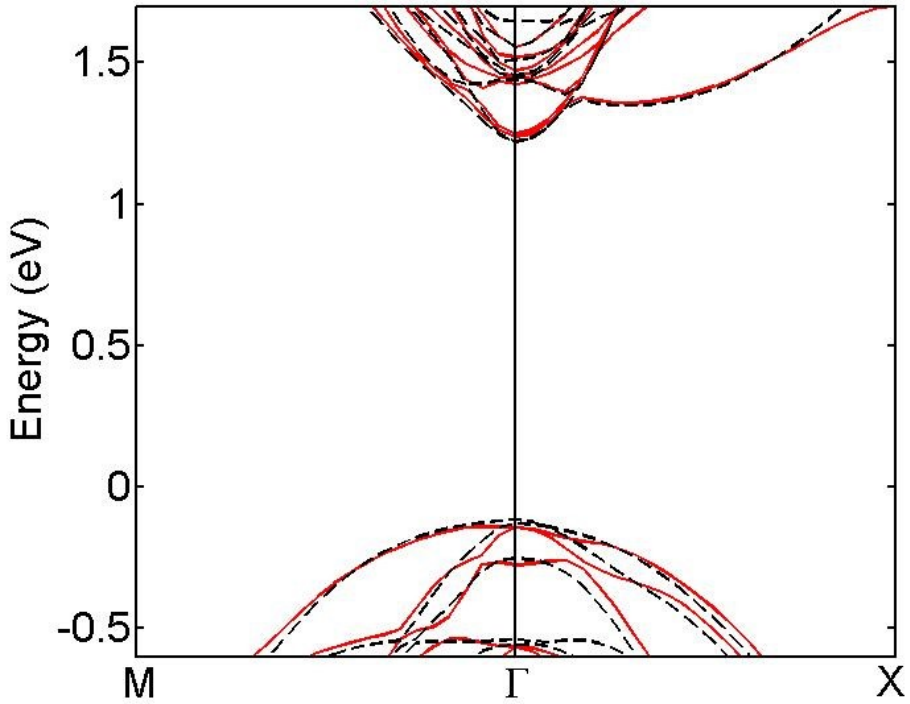
- Y. He, Y. Tan, Z. Jiang, M. Povolotskyi, G. Klimeck and T. Kubis,
  « **Surface Passivation in Empirical Tight Binding** »,
  in IEEE Transactions on Electron Devices, vol. 63, no. 3, pp. 954-958
- One doesn't want to include explicitely passivation atoms
- Preserve the original tight-binding structure of the device Hamiltonian
- Passivation acts as a supplemental **self-energy term**

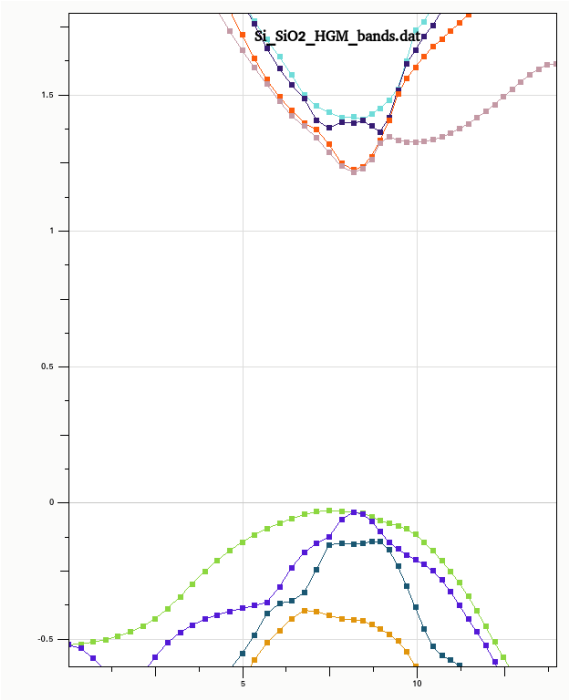
$$H_{SS} = H_0 + \lambda_P I + \sum_{P=1}^{N_{db}} \Sigma_{SS,P} \qquad \Sigma_{SS,P} = H_{SP}(\varepsilon - H_P)^{-1} H_{PS}$$

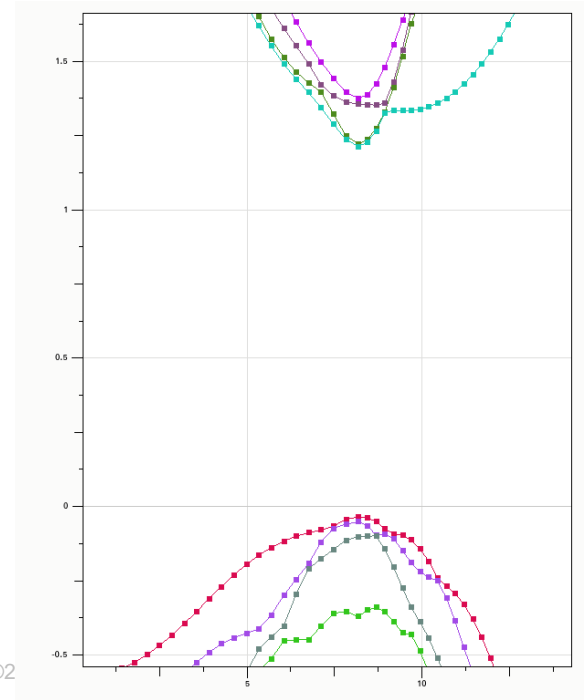
- Passivation (P) and coupling of P with Surface (S) terms and surface potentials are fitted
- The target is to reproduce a known BS obtained in ab initio (DFT + bandgap corr.)

Si <100> nm thin layer





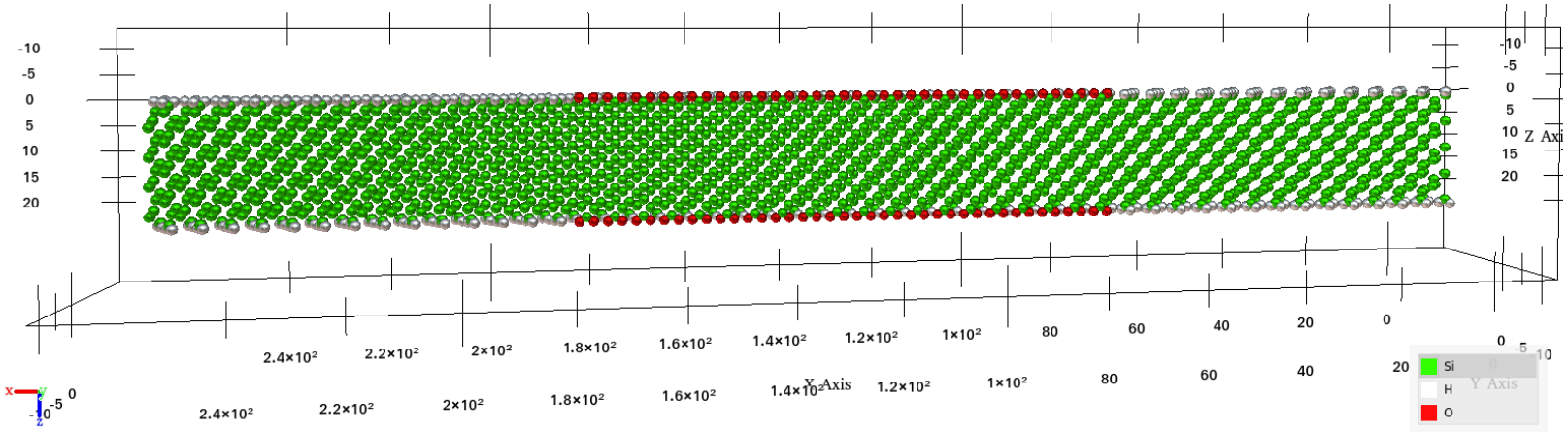


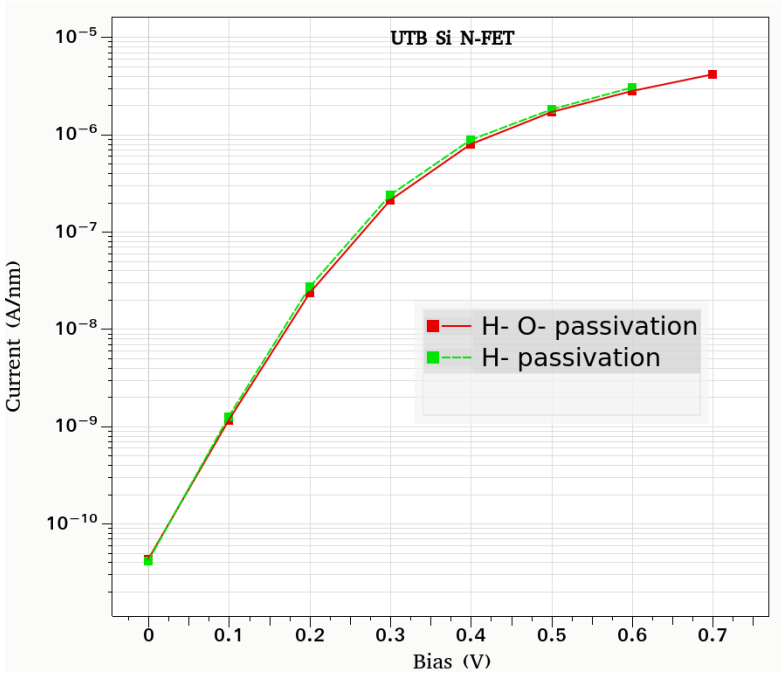


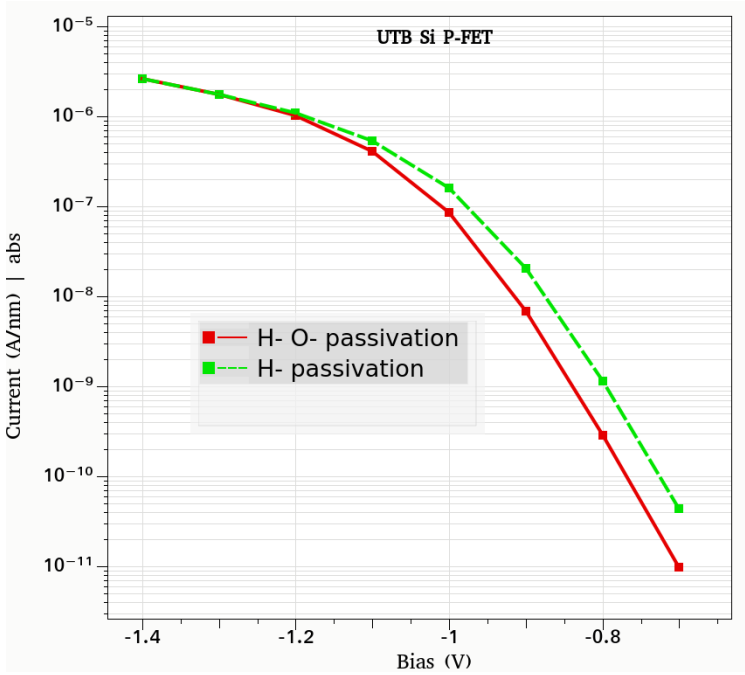
- TB parameters of O(s)-Si and H(s)-Si are fitted
- Reproduce the DFT BS for the first few bands below/above HOCO/LUCO respectively

UTB-Si Transfert Characteristic

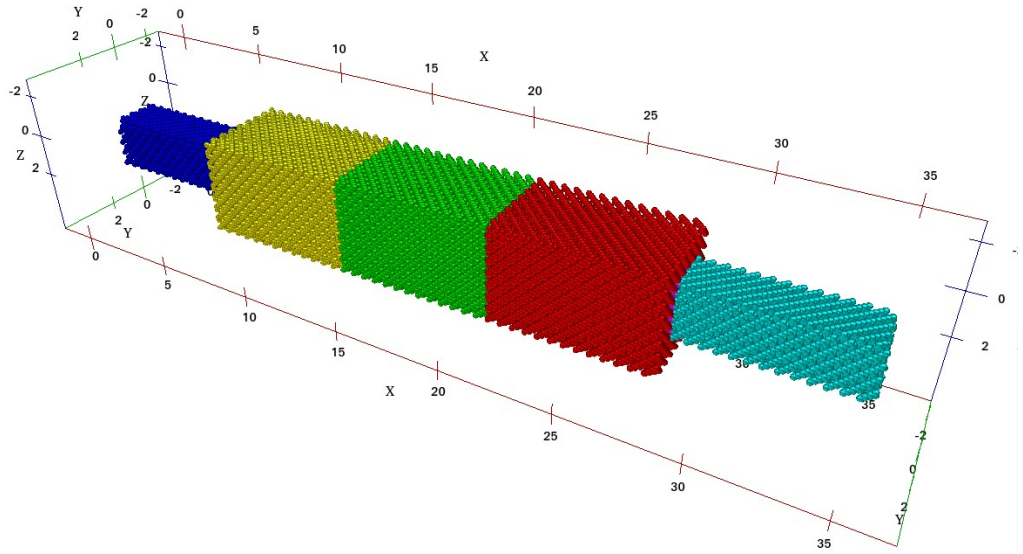
- Si <100>, t = 2.17 nm
- N-I-N & P-I-P UTB-MOSFET, 7 nm / 10 nm / 7 nm
- 1 nm EOT, Wf = 4.27 eV, N++/P++ = 10^{20} cm^{-3}
- Gate-oxide passivation ½ O ½ H
- Id(Vg), Vds = 0.5 V



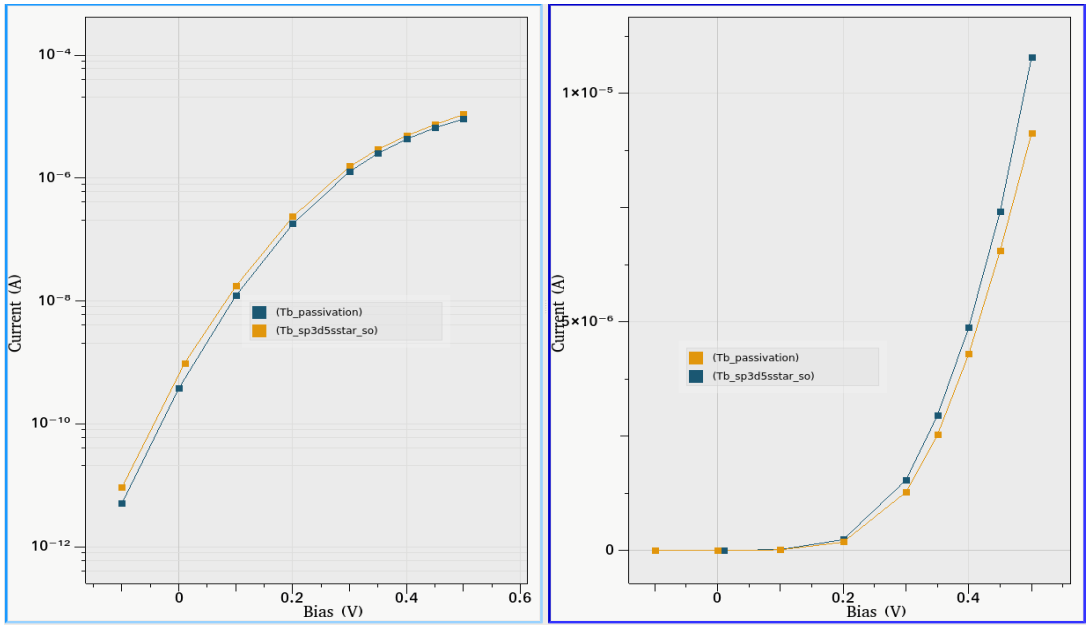


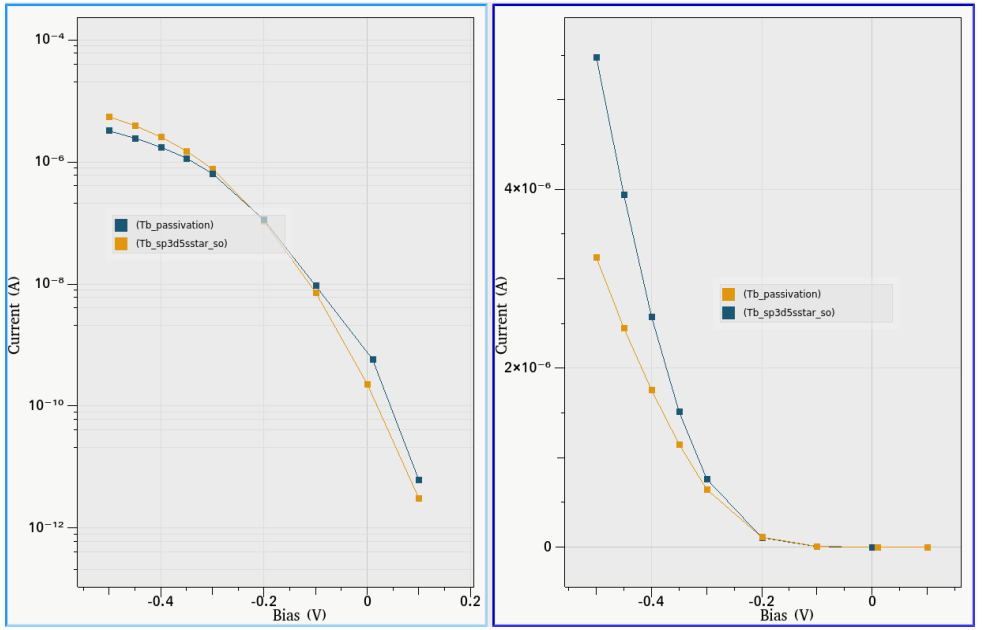


NWFET Characteristic



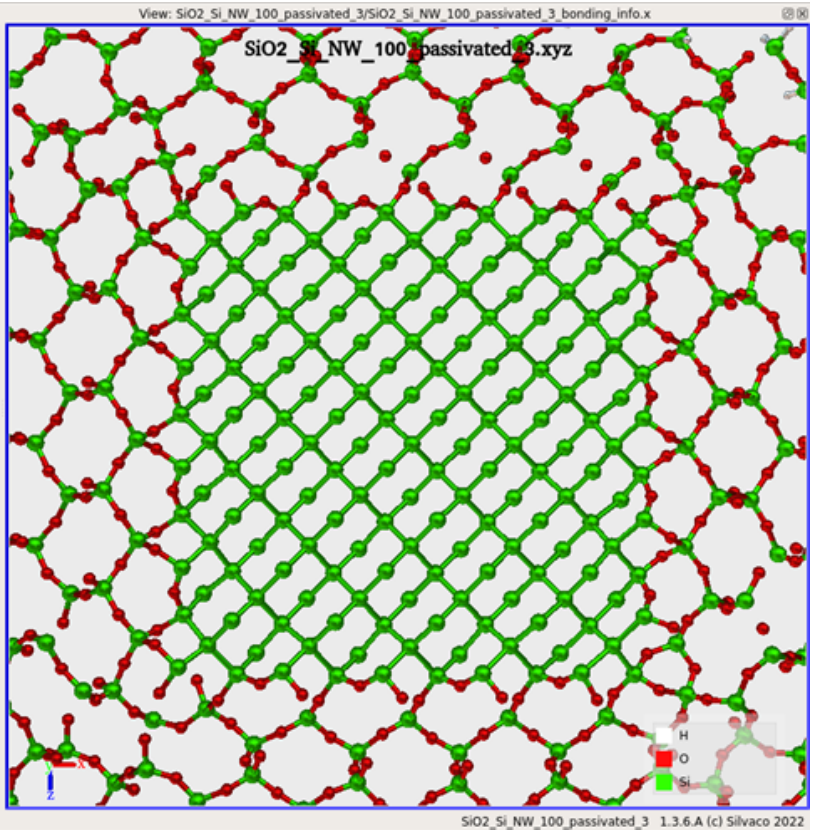
- Si <100>, 2.2x2.2 nm^2
- N-I-N & P-I-P NWFET,
  7 nm / 7 nm/ 7 nm / 7 nm / 7 nm
- 1 nm EOT, Wf = 4.27 eV,
  N++/P++ = 10^{20} cm^{-3}
- Gate-oxide passivation ½ O ½ H
- Id(Vg), Vds = 0.3 V

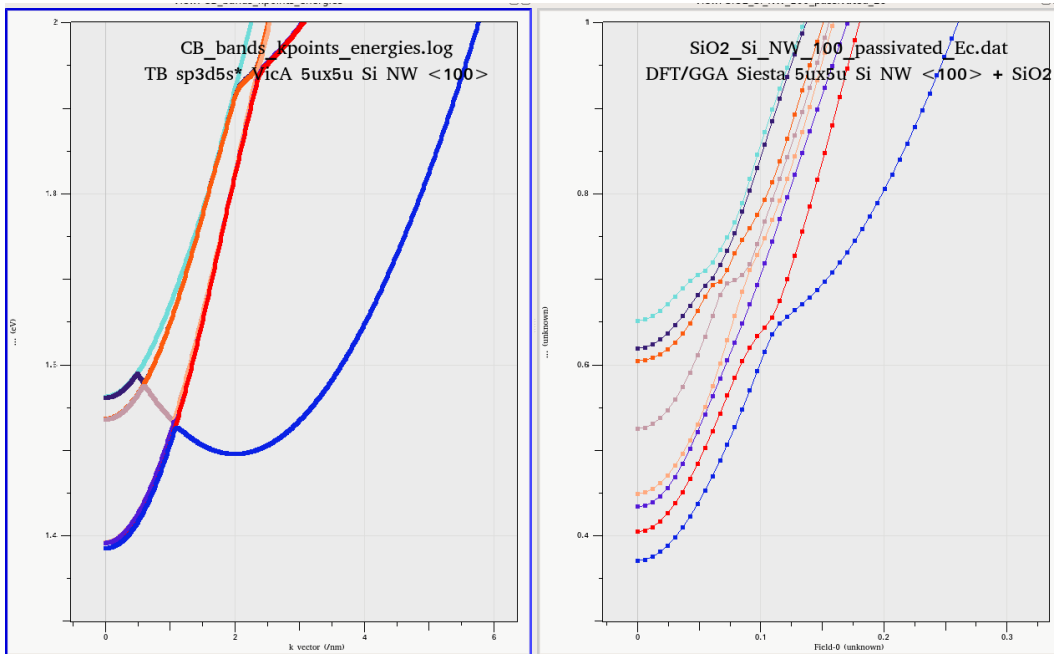


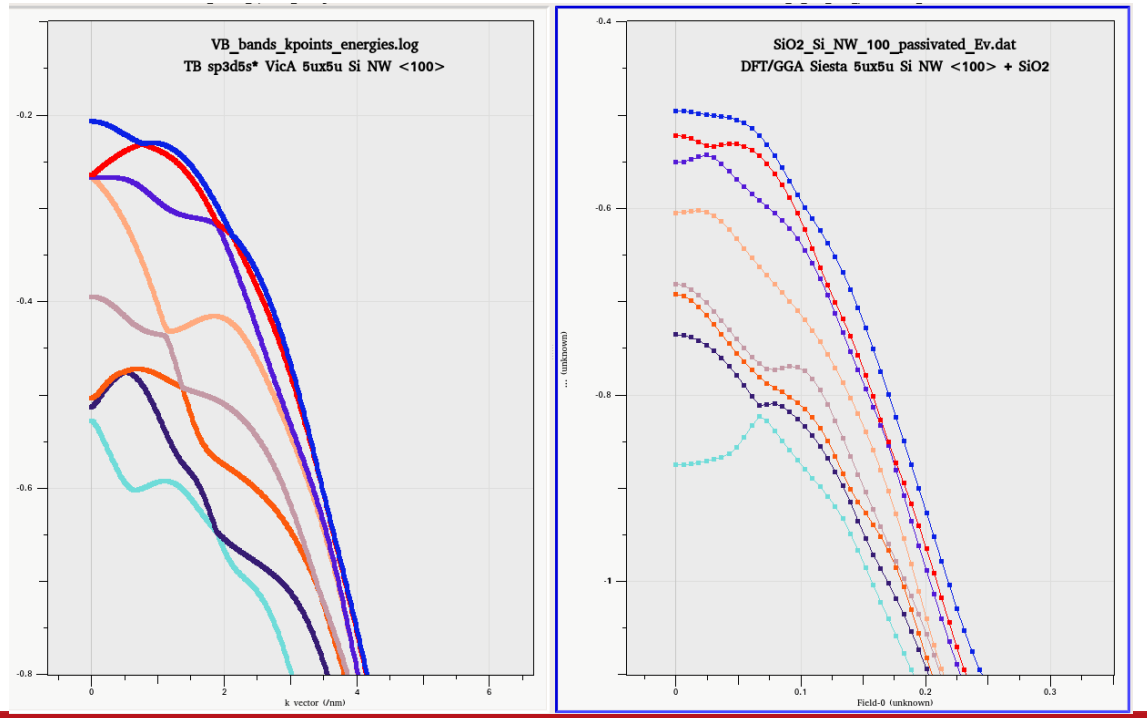


NWFET passivation, Si fully oxidized

- SiO_2 initial structure beta-cristobalite
- Si core is preserved
  First 2-layers of the NW are deformed
- No dangling bonds







Conclusion

- The silicon surface passivation needs to be considered when building the energetic landscape of a MOSFET
- The (Purdue) method of implicit passivation is light and allows to mimic of a distorted bandstructure due to oxidation
- The implicit method is compatible with RGF, modespace, and other self-energies
- Progress has to be made in order to include more complex oxide interfaces
- As it is, an engineer is able to elegantly introduce a source of MOSFET variability


Thank you
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