Unleash Innovation

# Where is semiconductor technology heading? A view from industry and implications on computational nanotechnology research.


Carlos H. Diaz

TSMC R&D


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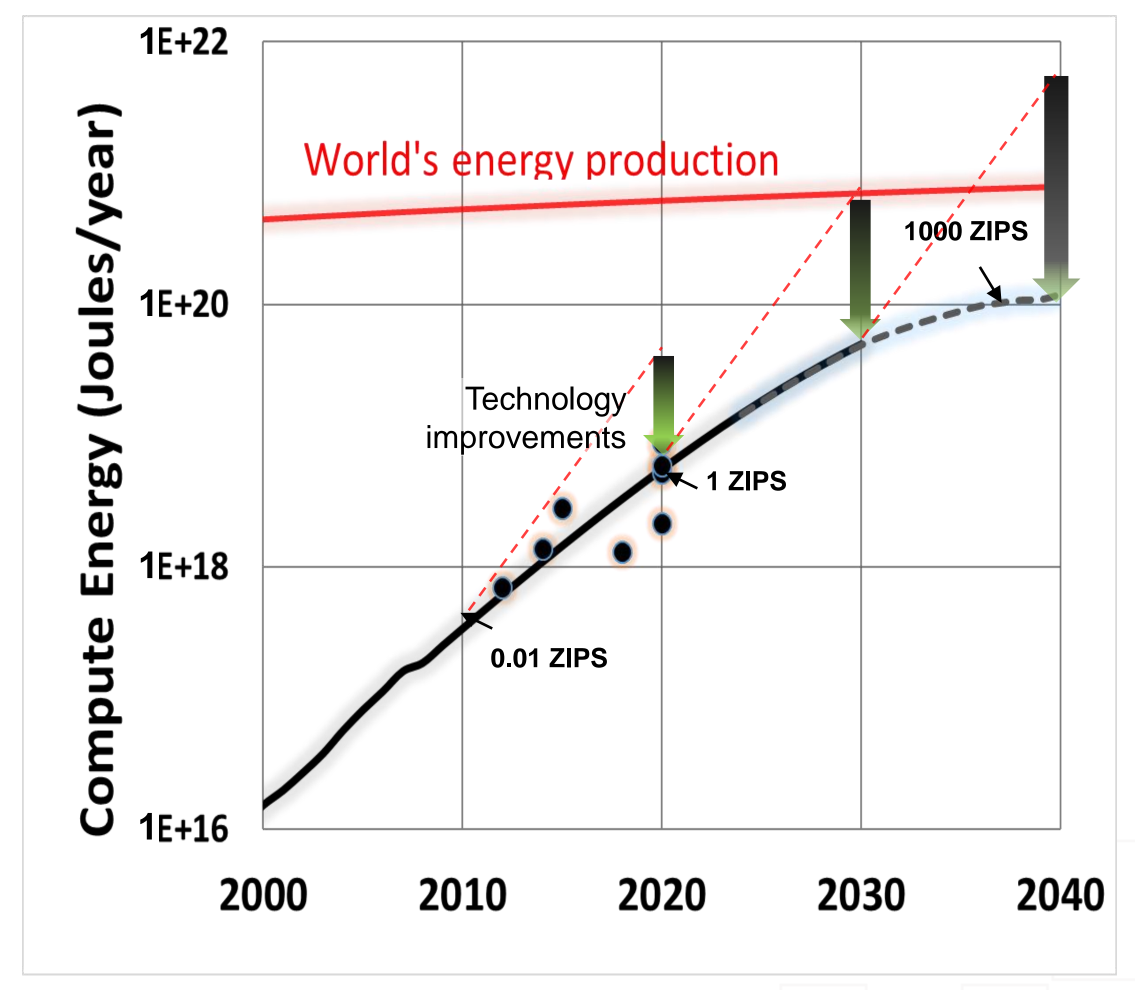
# Energy efficiency key for sustainable growth




SRC-SIA Decadal Plan for Semiconductors

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# Chip and System level Innovation

System-level

Chip-level

1961
The First Planar IC

A Few Transistors

1969

200 MOS Transistors

HKMG
Immersion
SD SiGe
Cu/LowK

7B Transistors

Thousands of Cores
28nm
2010

3D Fin-FET
2P2E
ELK
Low R barrier
Co cap liner

15B Transistors

More Cores
16FF
2015

New channel materials
EUV
Metal oxide ESL
Self-aligned line with flexible space
Low damage hardening / low-k and Novel Cu fill

>50B Transistors

Million Cores

CoWoS®

FPGA slice1
FPGA slice2
FPGA slice3

InFO®

150B Transistors

HBM HBM
Logic
HBM HBM

>300B Transistors

HBM HBM HBM
Logic
HBM HBM HBM

TSMC-SiOC™

Mark Liu, ISSCC 2021

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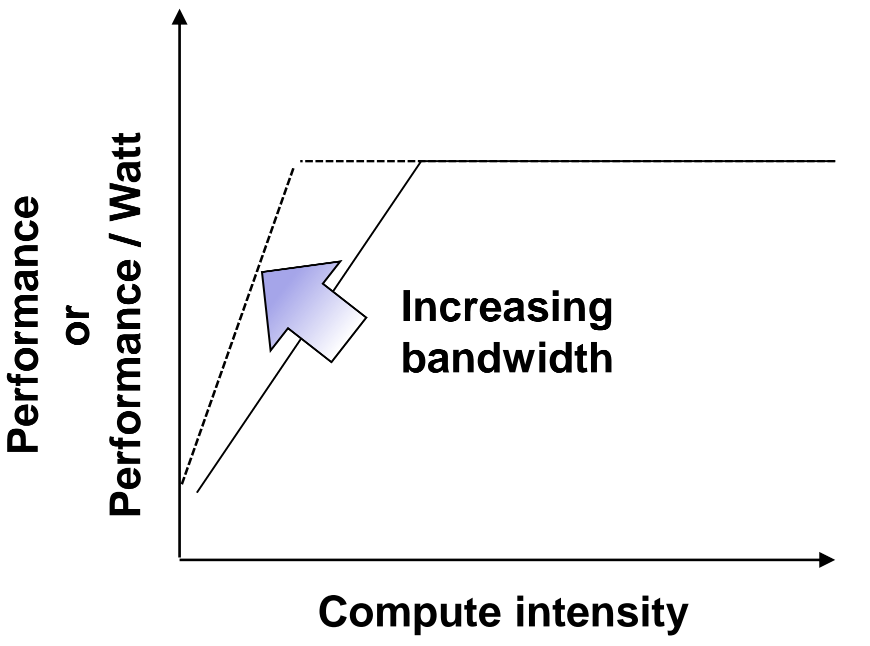
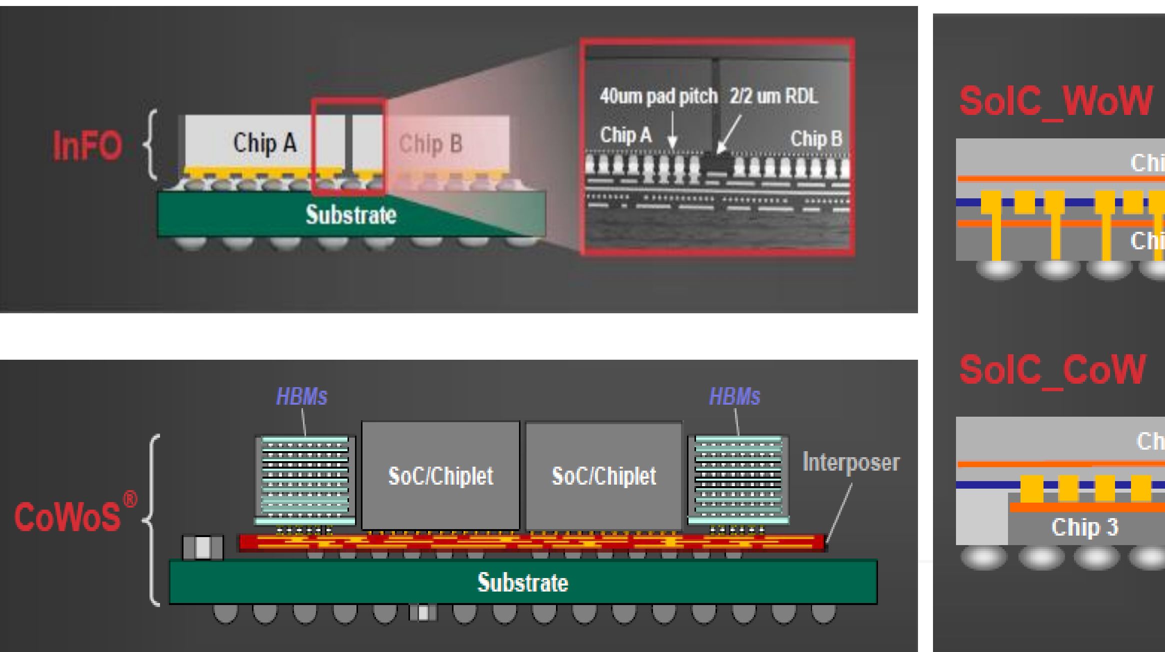
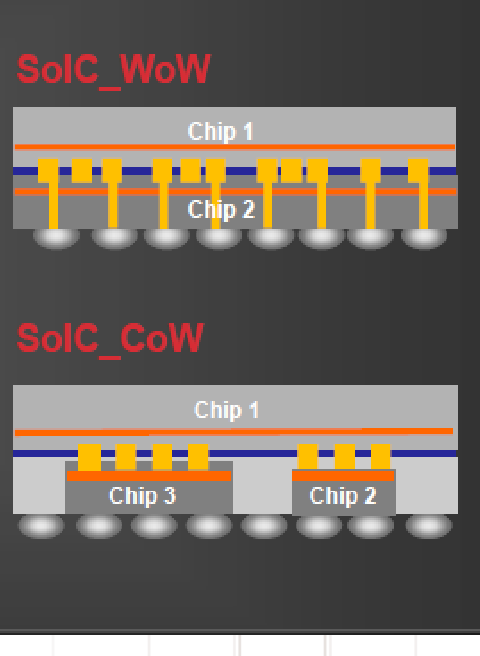
# System Integration Capabilities – TSMC 3DFabric™





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# 3D Interconnect Scaling for Higher Bandwidth

Bandwidth Capability

SoIC
Interposer
Fan-out
Flip-Chip
Other

Density ($mm^{-2}$)

$10^8$
$10^6$
$10^4$
$10^2$
$10^0$

SoIC

Interconnect Pitch (μm)

$10^{-1}$
$10^0$
$10^1$
$10^2$
$10^3$

1980 1990 2000 2010 2020 2030 2040

Year

Douglas Yu, ISSCC 2021

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# 3DIC modeling challenge & opportunities

- Discovering and developing fundamental insights with short TAT on materials & processes enabling sustainable cost-effective system integration growth in density, energy efficiency, performance, and reliability. -→ continuously pushing beyond SOTA
- Heat spreading and heat transfer
  - Film stacks – materials including their synthesis and interfaces
- Heat removal from nanostructures by conduction and/or convection
  - Exploration of materials and fluids, structures, interfaces, …
- Stress failure prediction and correlations to failure modes
  - Chip level, 3DIC level, and package-level
- Materials and processes for silicon photonics - waveguides, high-efficiency couplers, e-lenses, …

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# Transistors – Power supply scaling

- Breakthroughs needed to support decreasing gate-drive headroom
- New transistor structures, channel materials, and contact materials

Log (Drain Current)
Nanowire
Fin-FET
Planar
60 mV / dec
Steep sub-threshold FETs
Gate Bias (V)

VDD (V)
0.7
0.6
0.5
0.4
0
200
400
600
800
1000
1200
Average electron-hole mobility

Relative Power
N
N+1
N+2
N+3
VDD

# Transistor structural and integration trends

Planar → FinFET → Nanowires → Stacked FETs

Gate
Si
NMOS
gate
raised S/D
raised S/D
channel

SOURCE: semiconductor insights

STI

SOURCE: TECHINSIGHTS

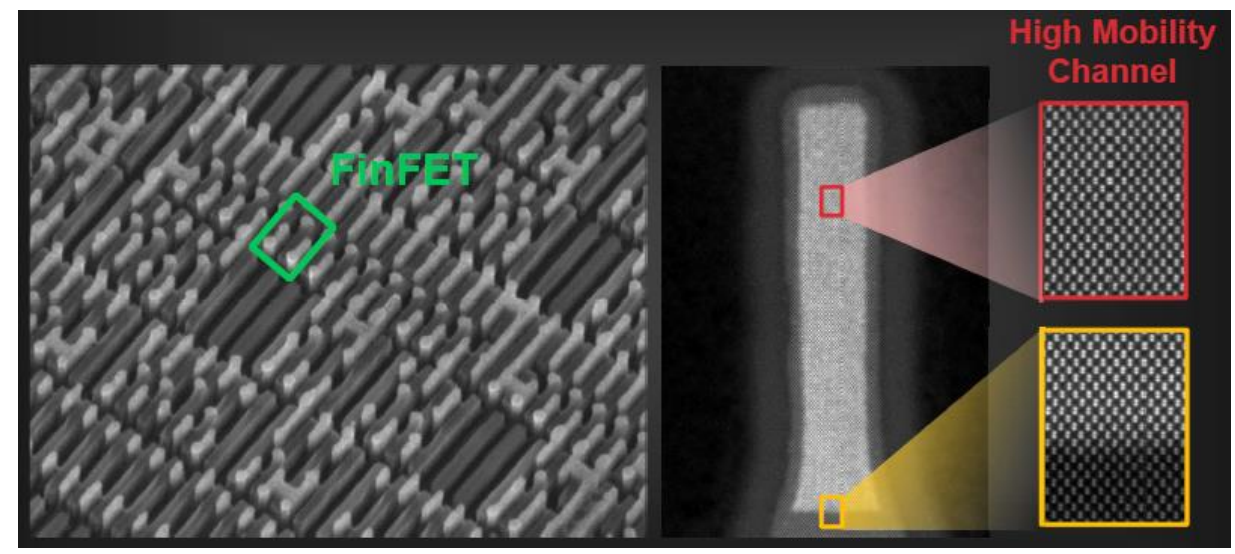
Gate metal

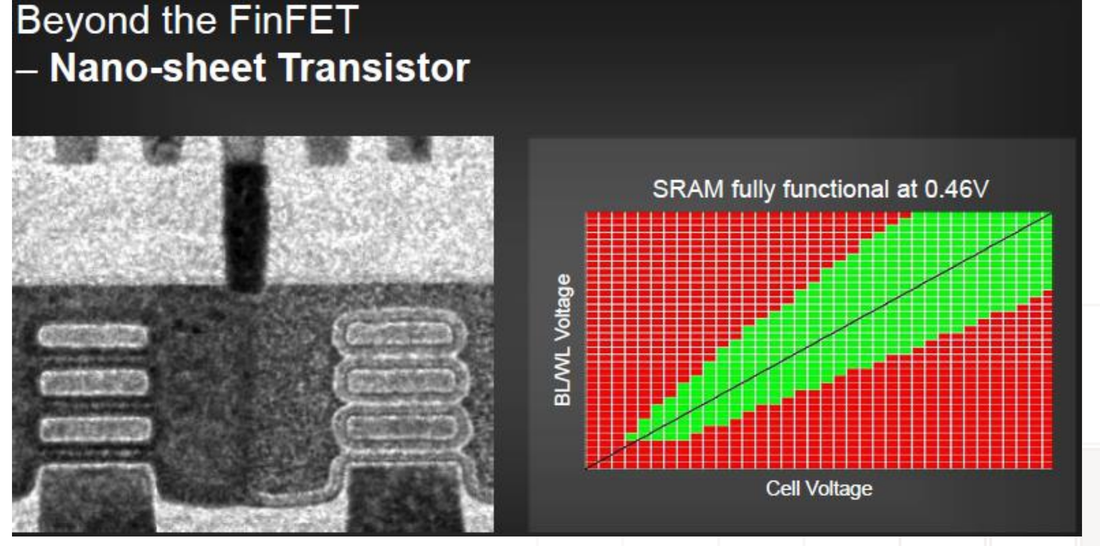
SOURCE: imec

Horizontal Routing
Contact connection
Drain (N)
Source (N)
Gate connection
Drain (P)
VSS
VDD

SOURCE: IMEC

# Transistor Materials and Structural Trends



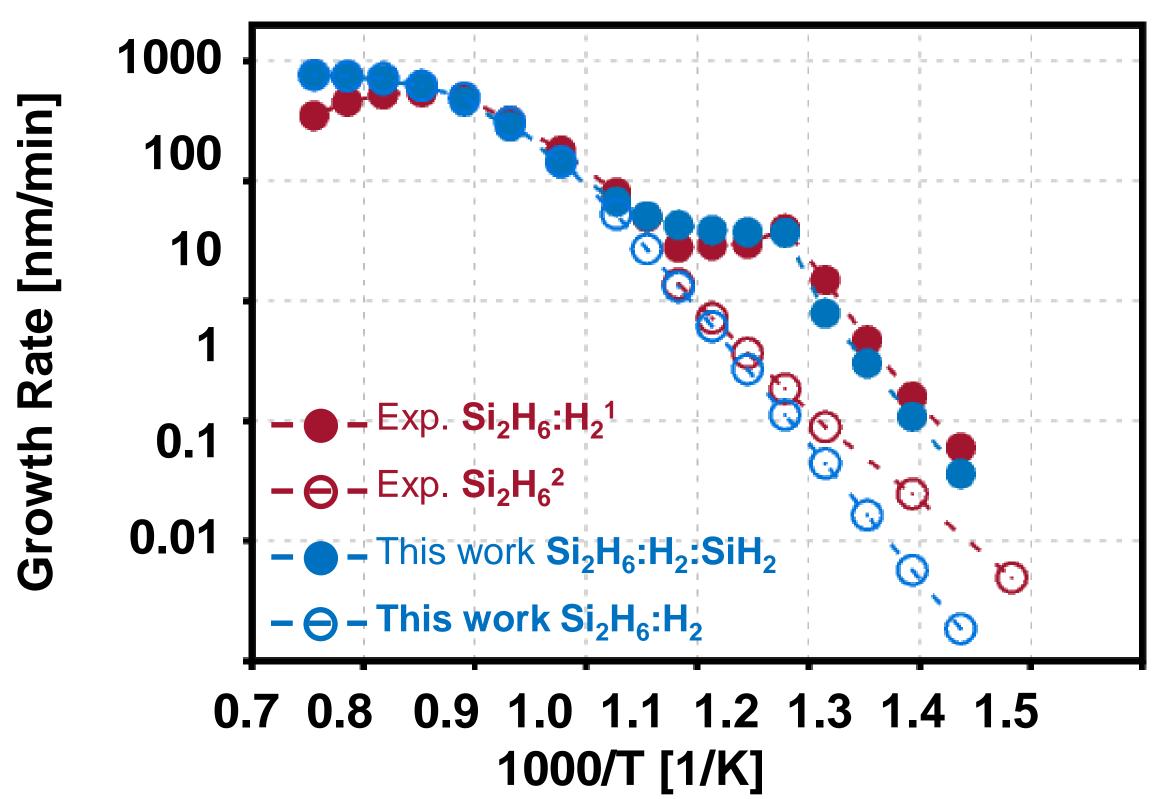




Mark Liu, ISSCC 2021

# Monolithic integration: modeling challenges & opportunities

- Predictive modeling for materials deposition or growth and etching processes to form high aspect ratio structures (devices or interconnect elements) with features in and/or out of line-of-sight
- Ditto for area (material)-selective deposition and etching – including surface functionalization chemicals and processes
- Accurate / predictive and fast TAT modeling in FEOL and BEOL
  - structural mechanical integrity through out the processes
  - self-heating and heat dissipation though the film stack from cell-level to die-level
- Stress failure prediction and correlations to failure modes

# A modeling case example for precursor absorption: new insights on Si Growth




| Reactions | Index | Activation energy or Feasibility[3] |
|---|---|---|
| $Si_2H_6 \rightarrow SiH_4 + SiH_2$ | R1 | ~ 2 eV |
| $Si_2H_6 \rightarrow H_2 + H_3SiSiH$ | R2 | ~ 2 eV |
| $SiH_2 + SiH_4 \rightarrow H_3SiSiH + H_2$ | R3 | Feasible at 740 K |
| $SiH_2 + Si_2H_6 \rightarrow Si_3H_8$ | R4 | Feasible at 740 K |
| $Si_2H_6 + H_3SiSiH \rightarrow Si_4H_{10}$ | R5 | Feasible at 740 K |
| $SiH_2 + Si_3H_8 \rightarrow Si_4H_{10}$ | R6 | Feasible at 740 K |

Ref. L. Li et al., IEDM 2022

[1] J. M. Hartmann, et al., *Thin Solid Films*, 2012, *520*, 3185
[2] D. S. Byeon, et al., *Coating*, 2021, *11*, 568
[3] K. Yoshida, et al., *J. Phys. Chem. A*, 2006, *110*, 4726

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# Beyond silicon-based channel: low-dimensional materials

Theory

T=300K

Mobility [$cm^2$/V-s]

Bandgap [eV]

ML $WSe_2$ $\mu_h$ $\mu_e$

ML $MoS_2$ $\mu_h$ $\mu_e$

ML bP

BL bP

Experiments

Bandgap [eV]

bulk $pWSe_2$

bP

Te

$PtSe_2$

bulk $MoS_2$

ML $WSe_2$ $\mu_h$ ($NO_2$) $\mu_e$ (Au,$Al_2O_3$, K) CVD $\mu_h$

ML $MoS_2$


[1] $WSe_2$, $WS_2$, $MoS_2$ from M. Luisier, IEDM 2016
[2] $WSe_2$, $MoS_2$ see also G. Gaddemane et al., IWCN, 2019, Z. Jin et al., and K.W. Kim et al., 2014 PRB, 2019 IWCN
[3] $WSe_2$ hole mobility: Prof. Chen/Purdue, Private comm.
[4] Graphene nano-ribbon from M. Fischetti, J. Physics, 2013
[5] Carbon Nanotube from X. Zhou, Phys. Rev. Lett., 2005

[1] P. Hashemi et al.," VLSI Tech. Dig., 2014.
[2] Z. Zeng, et al., IEEE TED, 2017.
[3] L. Li, et al., Nat. Nanotech., 2014.
[4] F. Xia, et al., Nat. Comm., 2014.
[5] H. Liu, et al., ACS Nano, 2014.
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[14] W. Liu, et al., ECE Trans, 2013.
[15] Z. Yao, et al., SISC 2017.
[16] M. Mleczko, et al., Sci. Adv., 2017.
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[18] J. Wu, et al., Nat. Nanotech., 2017.
[19] Y. Wang, et al., Nat. Elect., 2018.
[20] Y. Zhao, et al., Adv. Mater., 2017.


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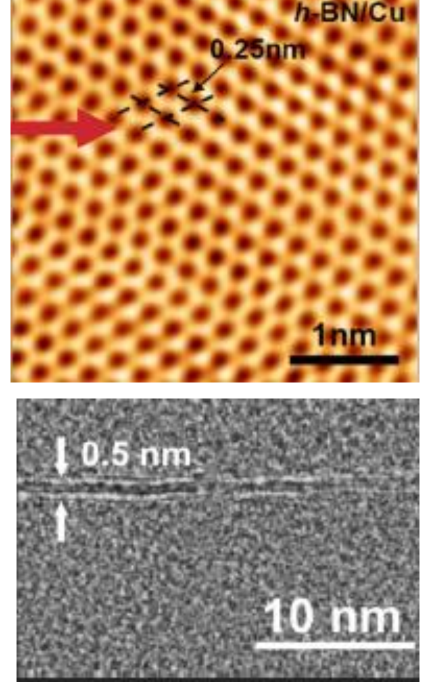
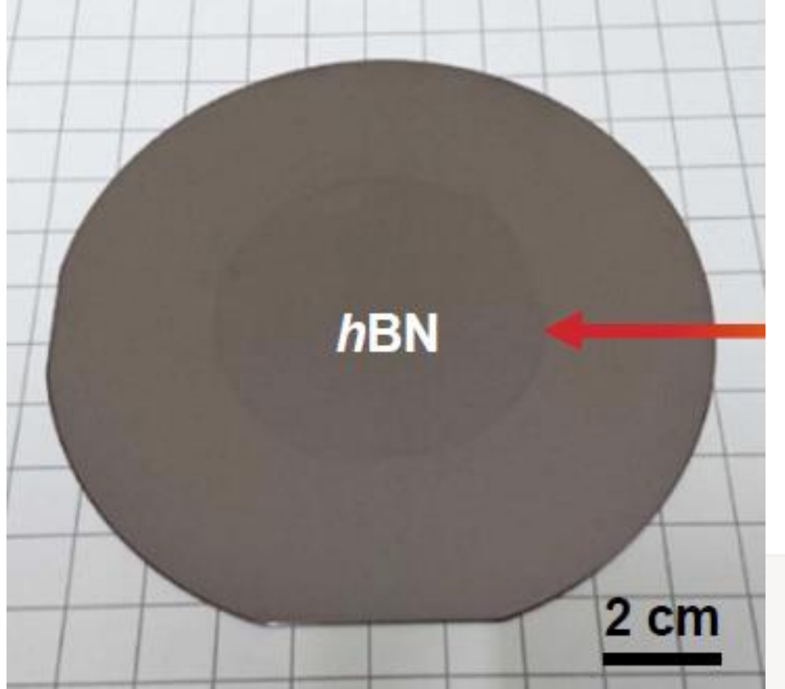
# 2D TMDs ($MX_2$) - channel and gate-dielectric materials

- M: a transition metal (W, Mo, …) and X: a chalcogen element (S, Se, Te)
- Wafer-level transfer-free high-quality channel material synthesis challenging
- Low-resistance contacts also challenging

Single crystal
monolayer h-BN as]
IL gate-dielectric layer




Wafer-scale
growth and transfer

T. -A. Chen et al., Nature, 2020

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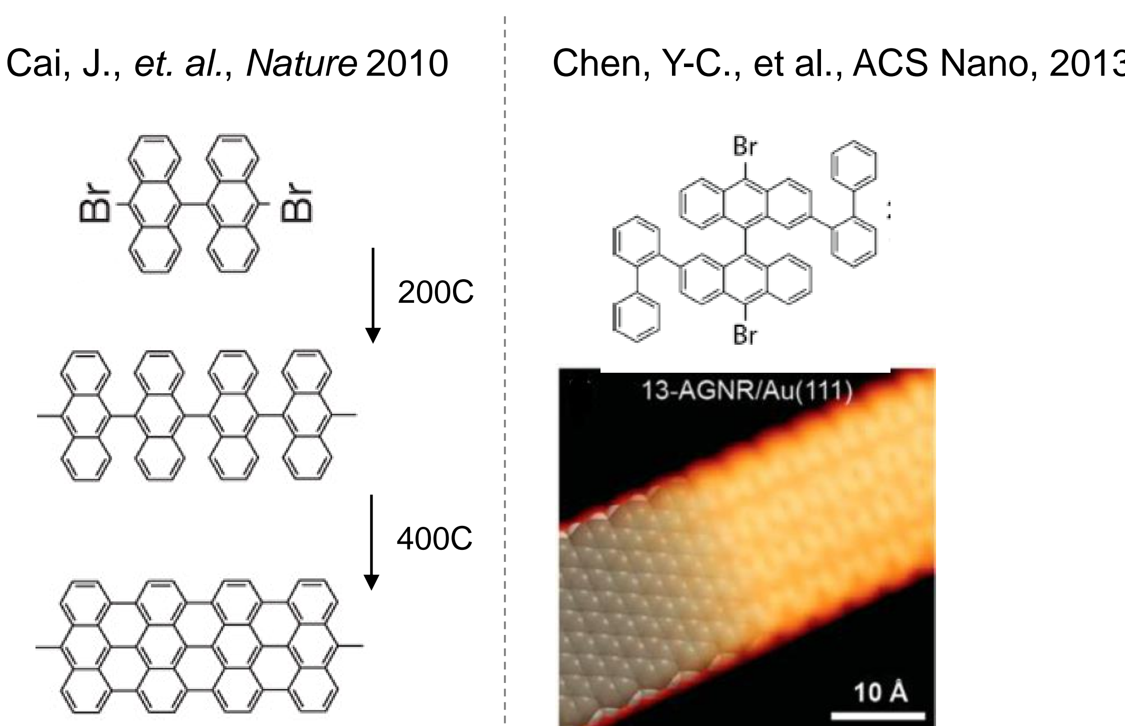
# 2D Channel materials: Graphene nanoribbons

- Progress being made on nanoribbons with defect-free edges

## Bottom-up molecular Synthesis

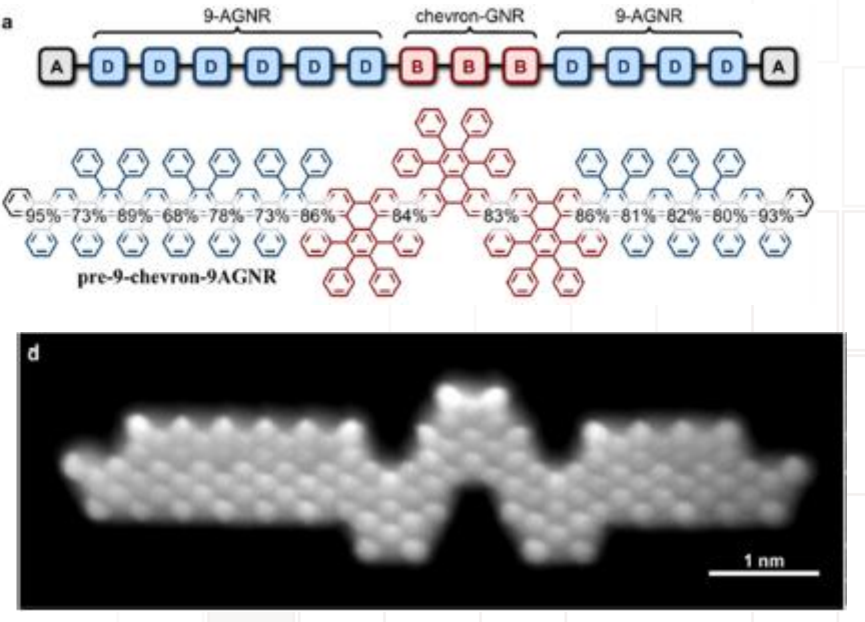
Cai, J., *et. al.*, *Nature* 2010

Chen, Y-C., et al., ACS Nano, 2013




## Molecular synthesis of heterostructures

J. Yin et al., J. Am. Chem. Soc. 2022, 144, 16012−16019



# 1D channel materials: Carbon Nanotubes

- Synthesis of oriented semiconducting CNTs is progressing

Horizontally aligned CNTs
Catalyst strips
Electric field

b

$CH_4$, 950 °C
Random nucleation
Fe catalysts
m-CNT
Junction
s-CNT
Carbanion

Electrostatic energy change:
$\delta E_{static}(t) = -q(t) \cdot E_{local}(t) \cdot \delta L$
$t_0$ :
Electric field
$t_0$

Reversal of electric field
Controllable renucleation
$t_1$ :
Electric field
$\delta L$
$t_0$ $t_1$

e
Without electric field
Mixed-CNT array
Growth direction
An ultralong CNT is placed
Catalyst strip

f
Twisting the helicity during the growth
An ultralong CNT is placed
s-CNT array
Mixed-CNTs
Catalyst strip

J. Wang et al., Nature Catalysis, 2018

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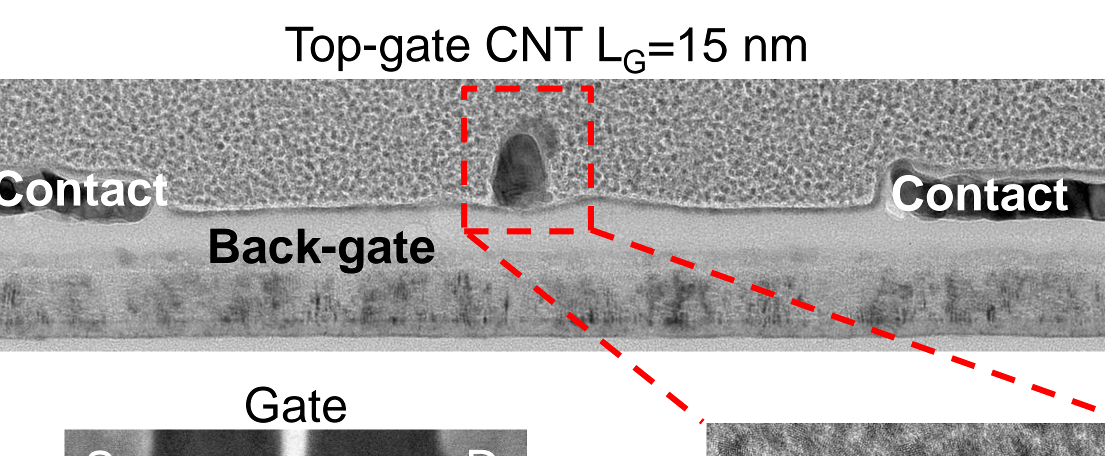
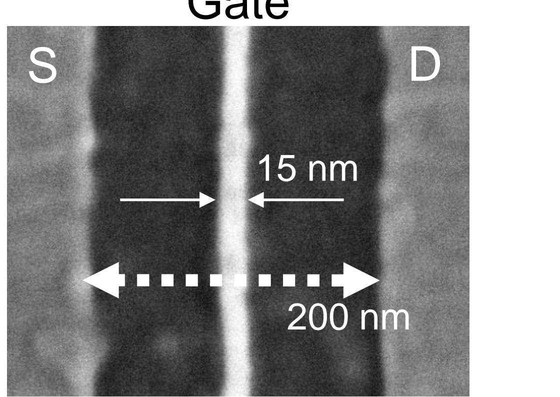
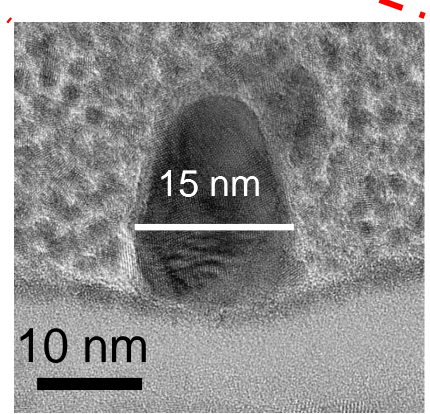
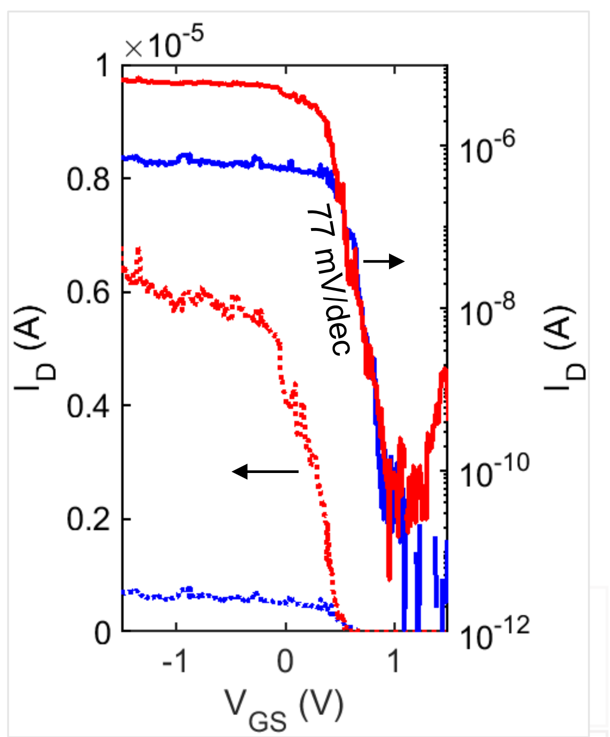
# Gate dielectrics for low dimensional materials

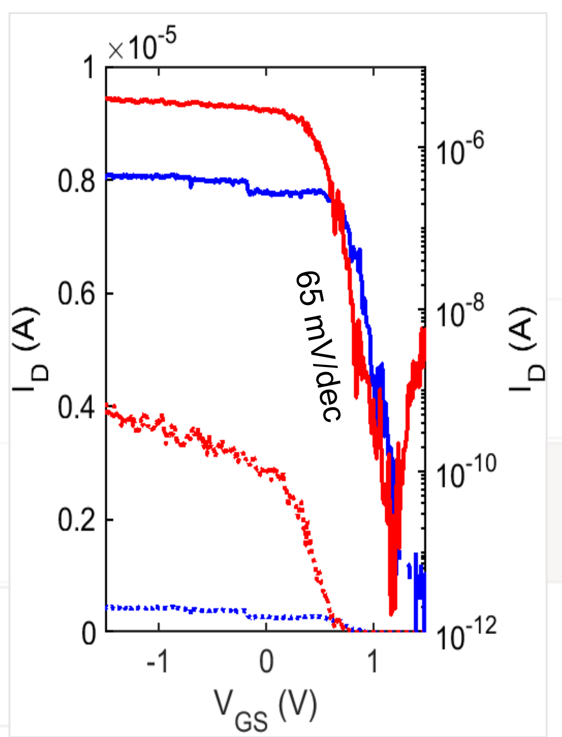
Top-gate CNT $L_G$=15 nm




G. Pitner et al., IEDM, 2020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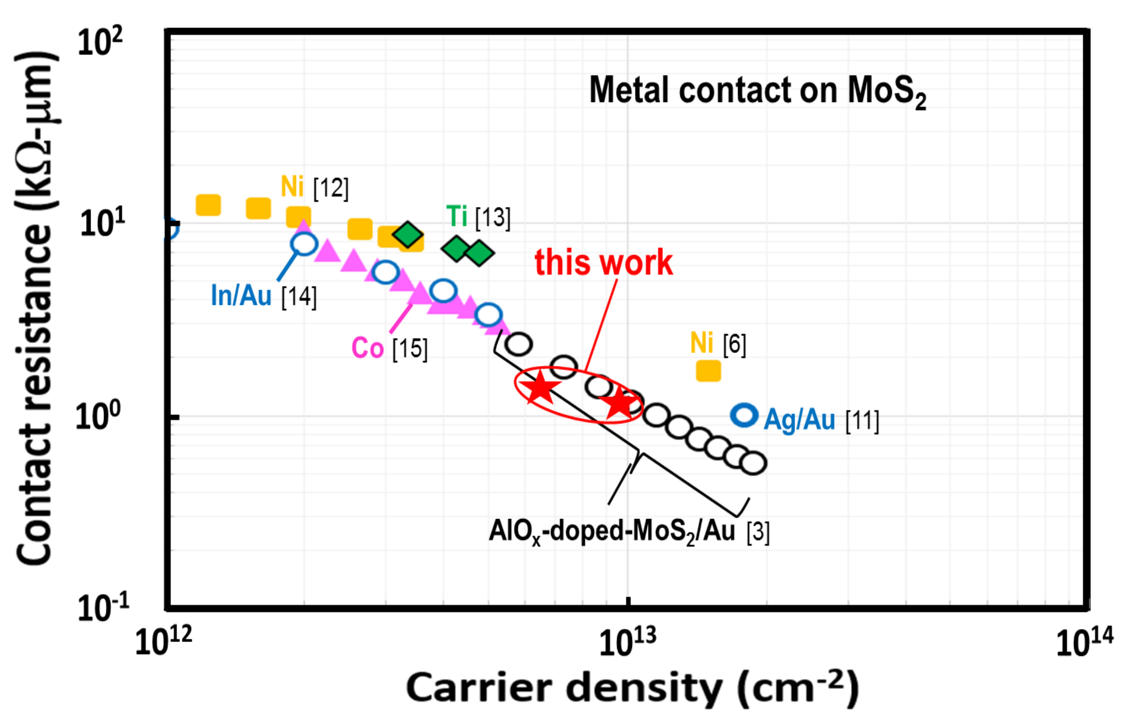
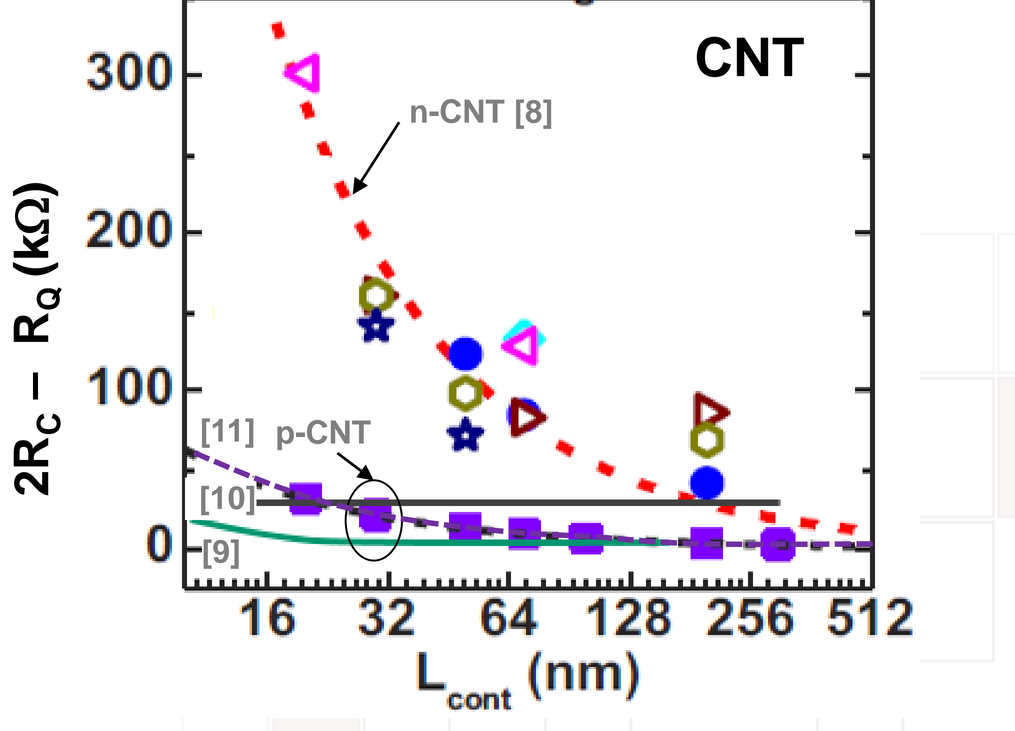
# Contacts for low-dimensional channel materials

- Challenges: Over 20X $R_C$ reduction, thermal stability > 400C, CMOS compatibility




A.-S. Chou et al., VLSI 2020




[1] Tang et al., VLSI Tech. Symp., 2017
[2] Pitner et al., Nano Letter, 2019
[3] Cao et al., Science, 2015
[4] A. Franklin, Nat. Nano, 2010

# Transistors: modeling challenges and opportunities

- Logic transistors
  - Comprehensive and predictive fundamental transport models that can realistically project on and off-state capabilities of devices having low-dimensional (2D or 1D) channels
    - TMDs, arm-chair graphene nanoribbons, CNTs
  - Ditto for thermally and mechanically stable low-resistance contacts to low-D channels
  - Accurate carrier scattering  in scaled devices - still opportunities @ fundamental level
  - Synthesis and processing of non-silicon based channel materials of device-quality
- Transistors for analog, mixed-signal, and other applications
  - Modeling of BEOL-compatible transistors – from materials & processes to transistor-level
    - e.g. GaN n & p-type transistors for CMOS, light sources and detectors for silicon photonics, …
  - Novel concepts with platform-relevant functionalities

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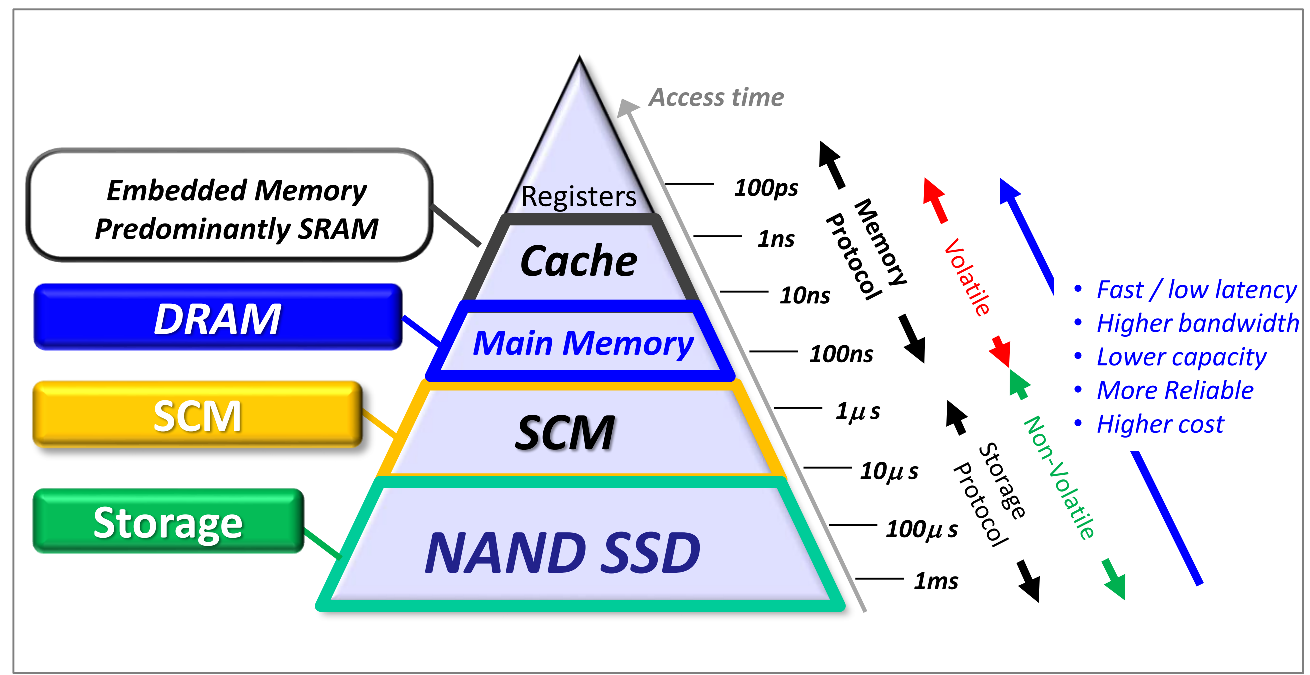
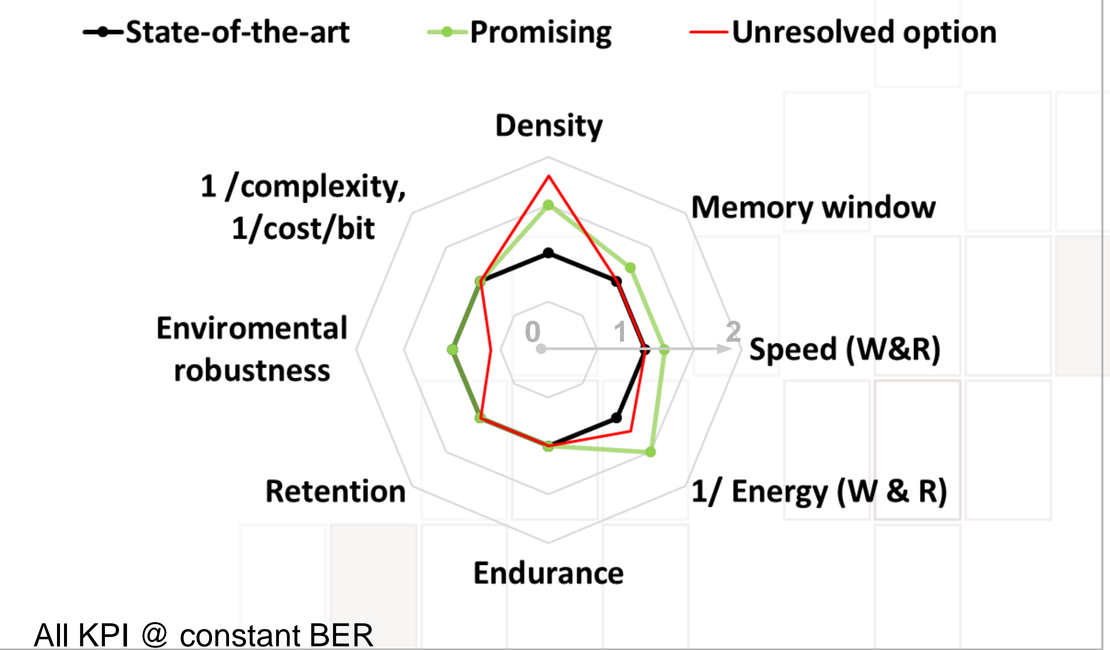
# New memory devices and key metrics

- Promising memory devices need to be uncompromising in all critical metrics compared to state of the art scaled solutions



# Spin-Transfer-Torque (STT) MRAM

- Benefits: Density compared to embedded SRAM or embedded Flash
- Challenges: Lower power & same speed / SRAM, magnetic immunity, thermal stability

Resistance

High R state "1"

Low R state "0"

Write Current

L. Thomas, MSST, 2017

Read Current

MgO

Write Current

$$P = A \cdot \frac{V_{c0}^2}{RA} = A \cdot RA \cdot J_{c0}^2$$

MTJ

Ru(7)
Ta(1)
CoFeB (1.5)
MgO
CoFeB(1.0)
Ta(0.3)
$[Co(0.4)/Pt(0.4)]_2$
Co(0.4)
Ru(0.42)
Co(0.4)
$[Co(0.4)/Pt(0.4)]_6$
Pt(5)
Ta(5)
$Si/SiO_2$ sub.

Free layer (recording layer)

Reference layer (Pinned layer)

S. Ikeda et al., IEEE IEDM 2014

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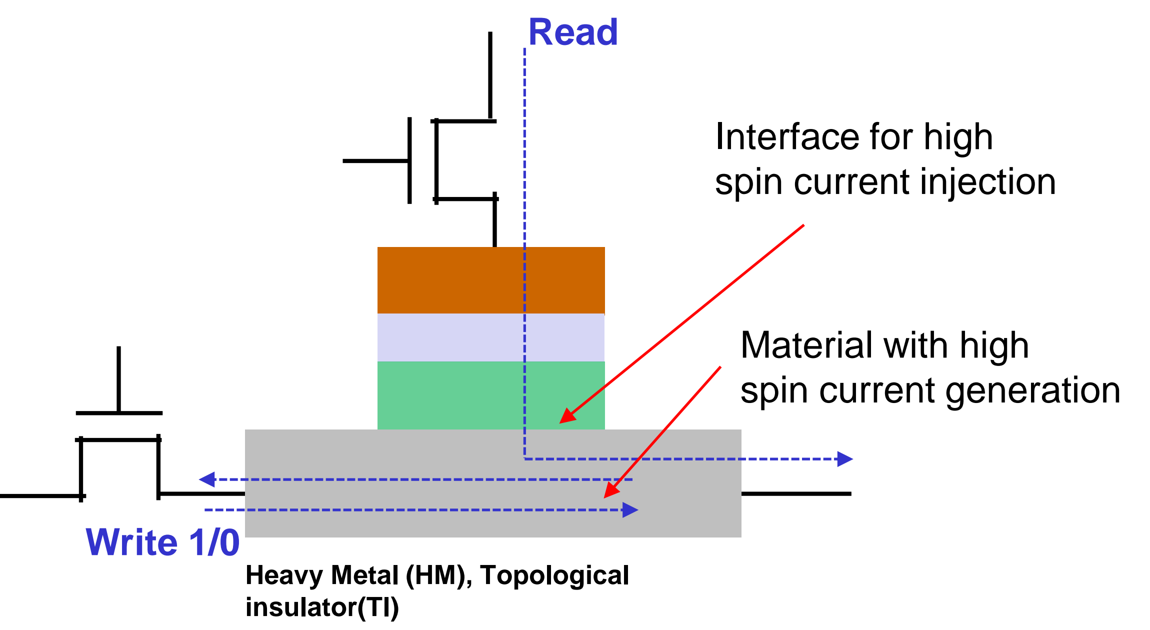
# Spin-Orbit-Torque MRAM potential

- Low power, high speed, higher R/W margin, and higher endurance versus STT-MRAM
- Challenge: attain benefits with cell-size significantly better than 6T-SRAM
- Type-Y cells remain most promising albeit density benefits lesser versus X or Z




$$P = RI_{c0}^{2} = \frac{\rho}{wt} \cdot I_{c0}^{2} = \rho \cdot t \cdot J_{c0}^{2}$$

| Type-Y (1, 3, 4) | Type-X (3) | Type-Z (2, 5) |
|---|---|---|
| FL, $J_e$, HM | Hz | Hx |
| **Field-free** | Not field-free | Not field-free |
| $J_C$ ~10 MA/cm² (3) | ~40 MA/cm² (3) | ~100~300 MA/cm² |


1. S. V. Aradhya et. al. Nano Lett. 2016, 16, 5987−5992. - Cornel
2. M. Cubukcu et al, IEEE ON MAGNETICS, VOL. 54, NO. 4, 2018 - CEA
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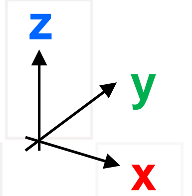
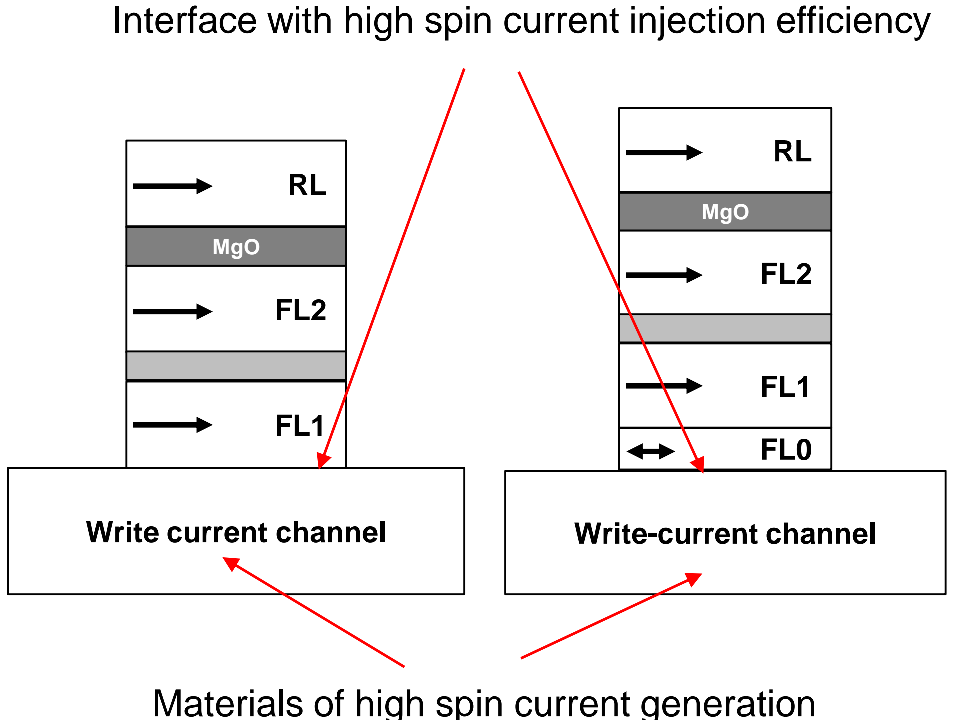
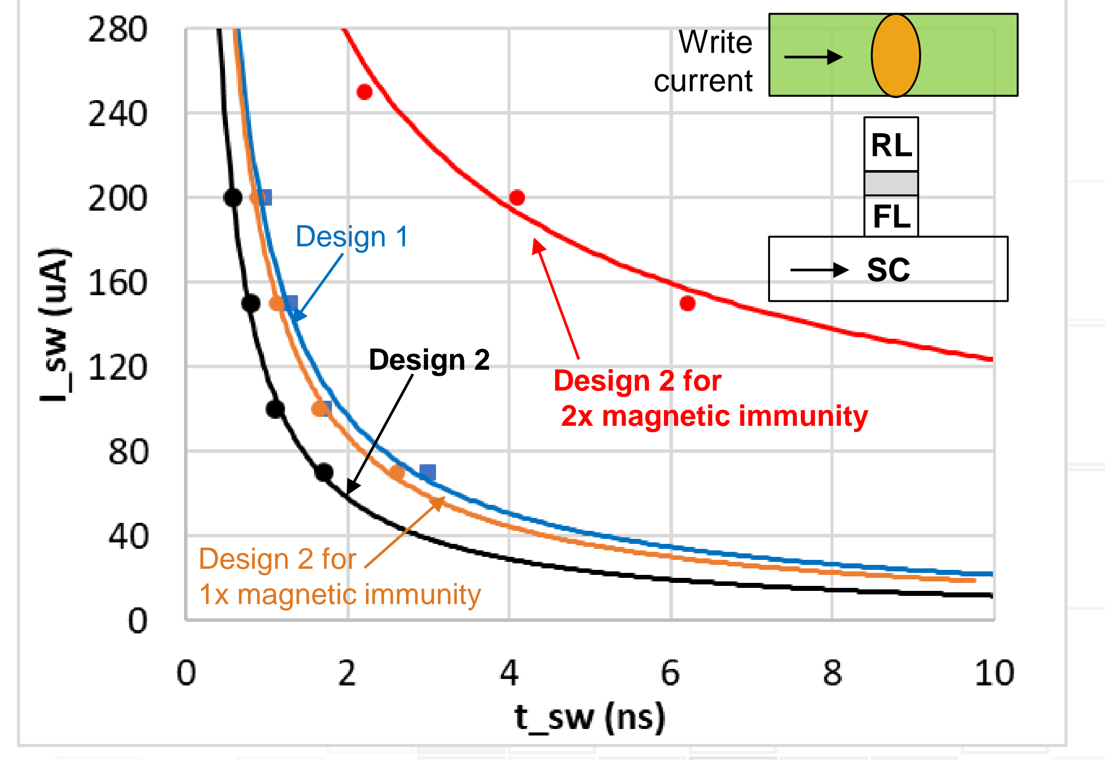
4. Zhu et. al. Adv. Electron. Mater. 2020, 6, 1901131 - Cornel
5. Kevin Garello et al. IEDM 2019 - IMEC

# SOT-MRAM

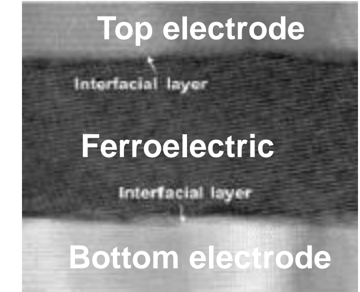
- Write path material & interface yielding high injected spin currents into FL are key to low power
- Free-layer and write-channel co-design key to low switching current & magnetic immunity

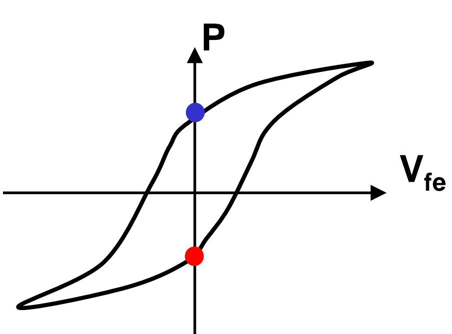


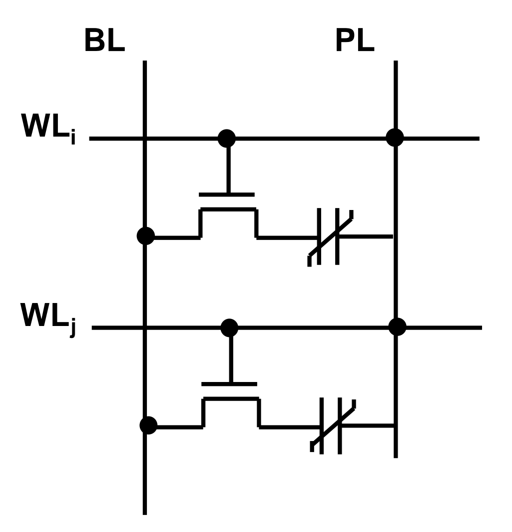



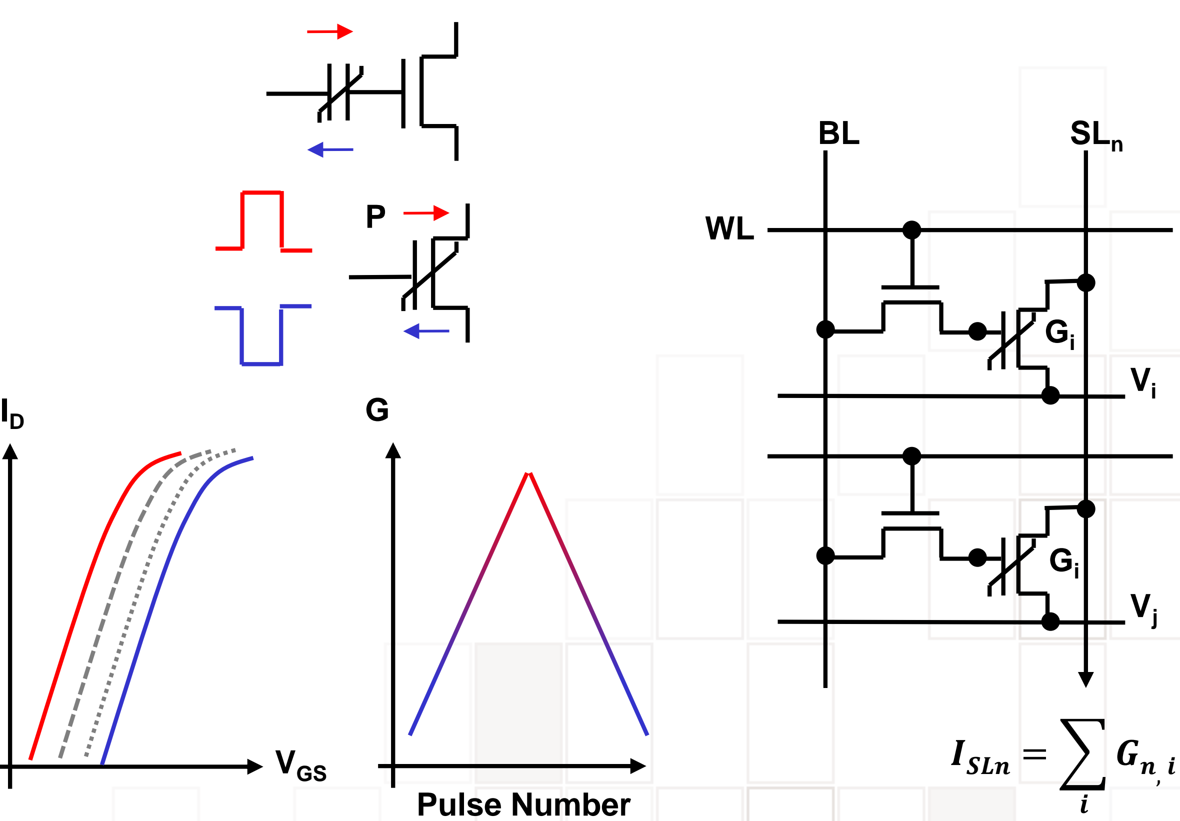
# Ferroelectric Memory – 1/2

- Ferroelectric memories primary benefits include density, low power, and speed.
- Challenges: endurance, retention, leakage and voltage scalability
- Possibilities: MLC capability

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# Ferroelectric RAM (MFM) – 1/2

- Electrode materials and interface layers along with ferroelectric film quality are all critical to ferroelectric device endurance – innovation opportunities

Bipolar Cycling Stress

Pristine | Redistribution | $V_O$ Generation

TE, $V_O$, BE

| | TaN | Ru |
|---|---|---|
| $E_{int}$ | -0.17 | -0.12 |

TaN/HZO/TaN
Ru/HZO/Ru

Polarization ($\mu C/cm^2$)

Electric Field (MV/cm)

Ru/HZO/Ru,
Low-field cycles, +/-1.75MV/cm
High-field cycles, +/-3.5MV/cm

T=+25°C
T=-40°C

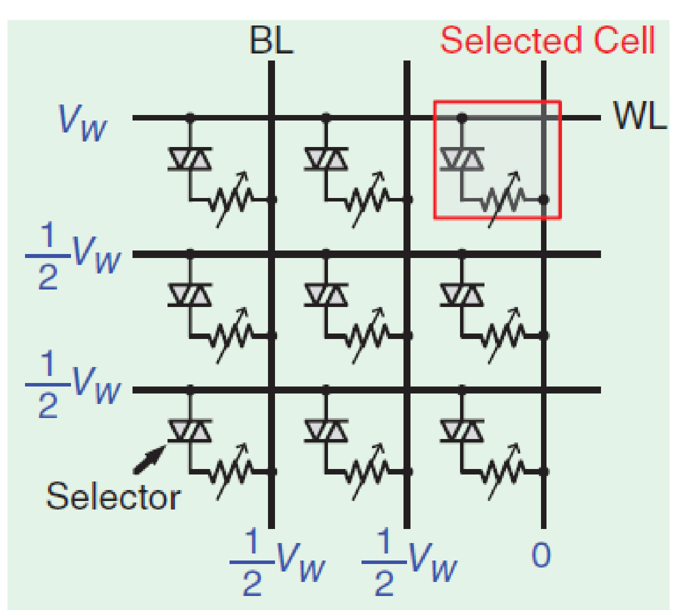
$2Pr / 2Pr_0$

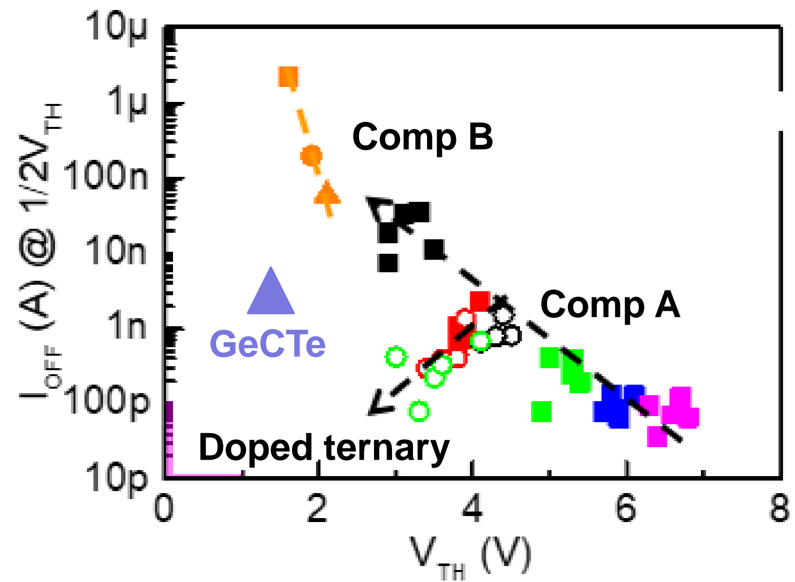
Cycle (#)

P. J. Liao et al., VLSI, 2020

# Cross-bar memory arrays

- Cross-bar arrays have benefits in memory cell area and array-efficiency
- Selector devices with sub nA leakage, on-state current ~1mA, and high speed are key
- Challenges: voltage scalability, thermal stability, variability, drift, endurance, ESH friendly material solutions




| Material | $V_{TH}$ | $V_H$ | $I_{OFF}$ | $I_{ON}/I_{OFF}$ | Endurance |
|---|---|---|---|---|---|
| SiGeAsTe [9] | 2.5V (1µs) | 1.2V (1µs) | 0.9nA (0.5V) | 5.6x$10^5$ | $10^{11}$ (1µs) |
| CTe [5,6] | 0.8V (250ns) | 0.36V (DC) | 9nA (0.4V) | $10^5$ | $10^8$ (250ns) |
| BTe [6,7] | 1.3V (1µs) | 0.5V (DC) | 10nA (0.5V) | $10^4$~$10^5$ | $10^8$ (500ns) |
| SiTe [8] | 1.0V (AC) | 1.0V (AC) | 100nA (0.6V) | $10^3$ | $10^8$ (150ns) |
| GeCTe (This work) | 1.32V (10µs) | 0.62V (10µs) | 3nA (0.5V) | $10^4$ | $10^{11}$ (500ns) |

Y. S. Chen et al., VLSI, 2021

# Memories: modeling challenges & opportunities

- Accurate and fast TAT “tail-bit” and device-to-device variation prediction
  - Enabling design-space exploration including process variability effects
  - Enabling DTCO in terms of PPA, bit error rates, retention, endurance, …
- Endurance and cycle-to-cycle variation prediction using reliability physics
  - TDDB at MgO layer in an MTJ
  - Fatigue, imprint and SILC effects in an Fe-FET
- Screening of new materials using ab-initio level models:
  - High spin polarization generation and transport in an MTJ
  - High quality interfaces for gate stack in an Fe-FET

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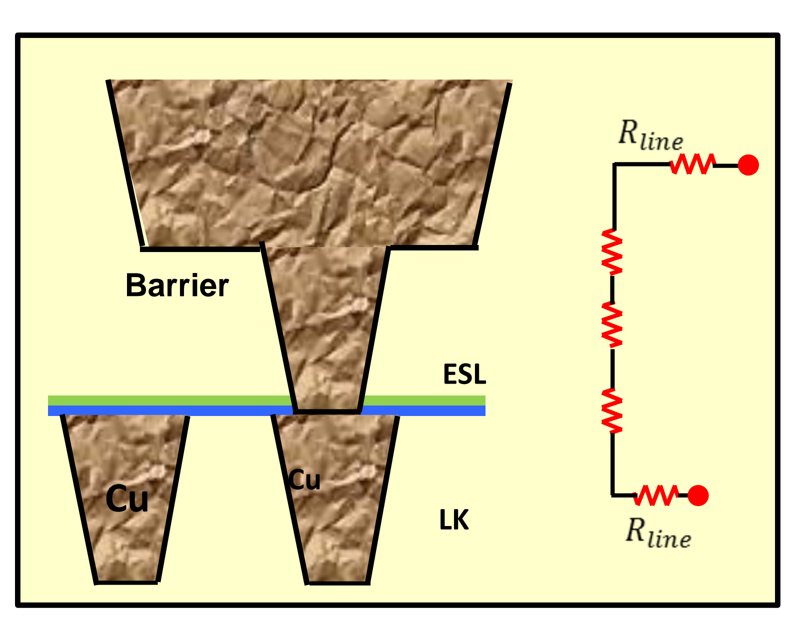
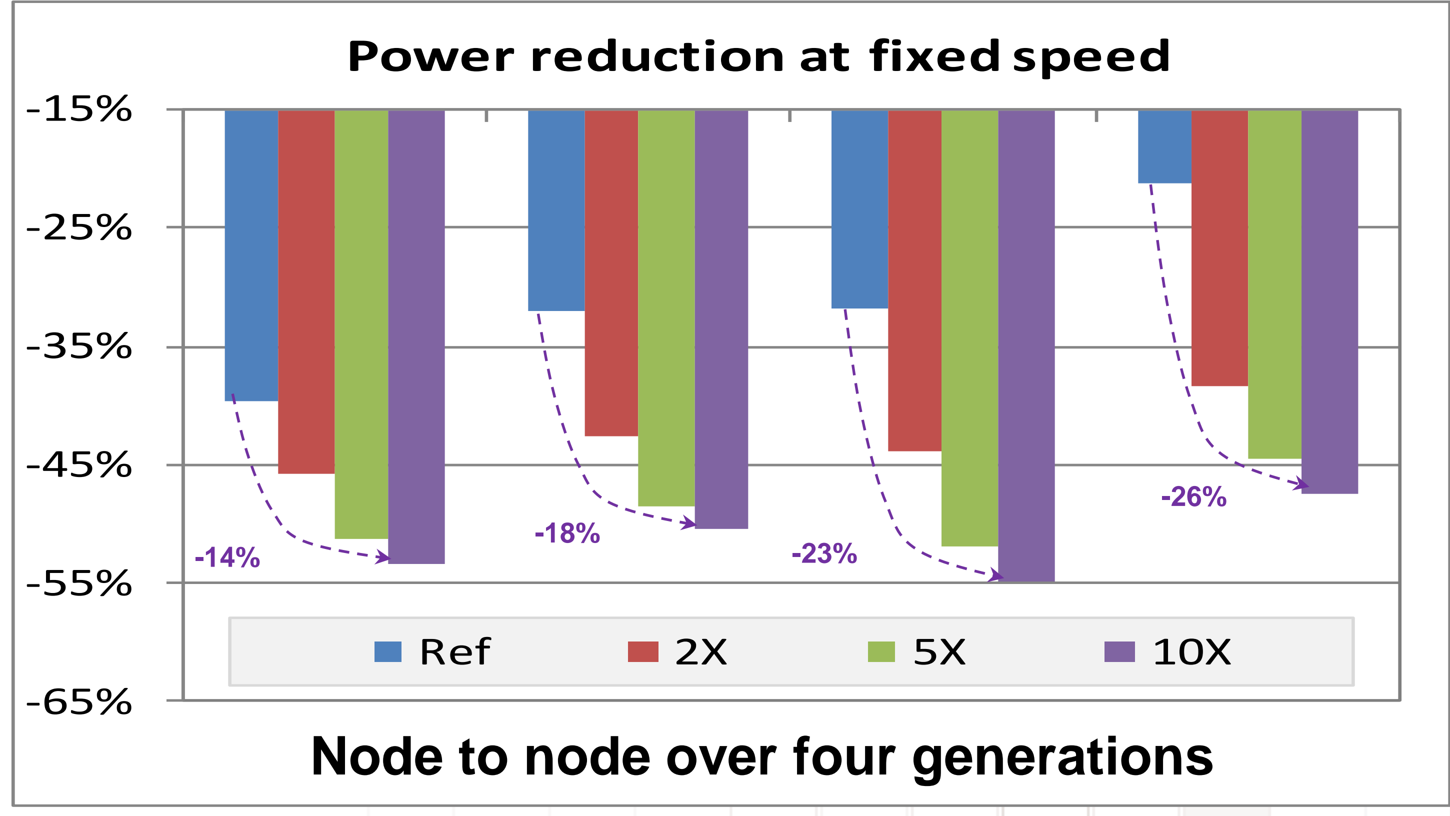
# Interconnect resistance challenge

- New thinner metal barrier materials continue to key for low-R vias and lines
- Need materials enabling > 2X line & via resistance reduction / Cu

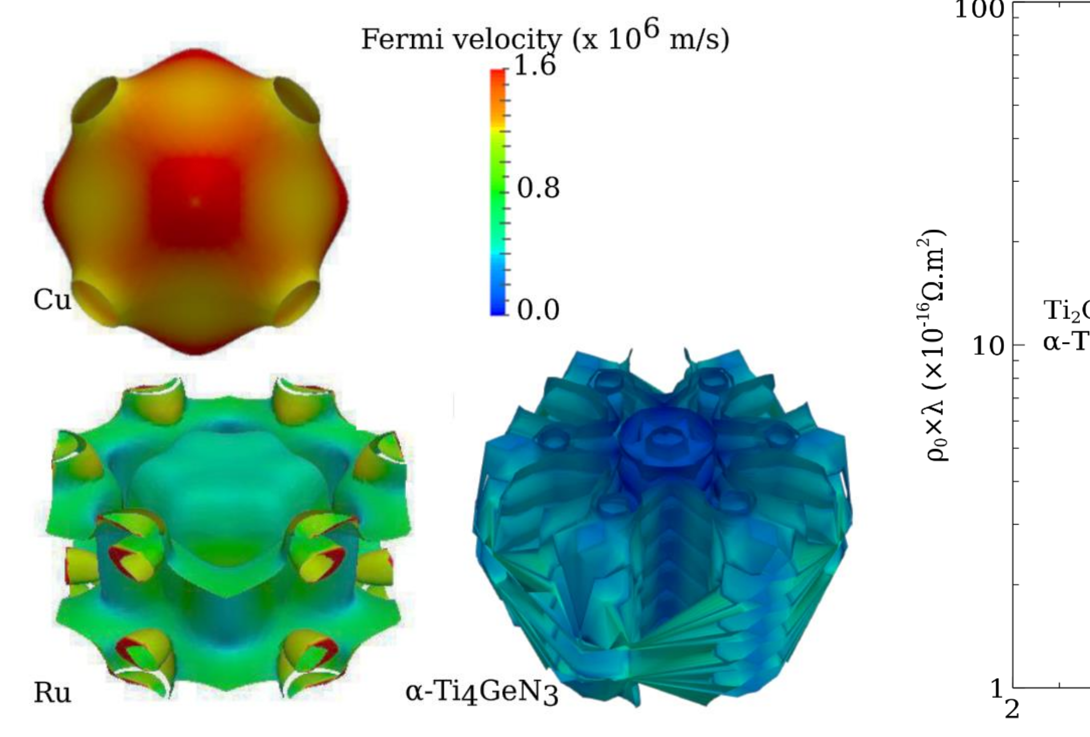


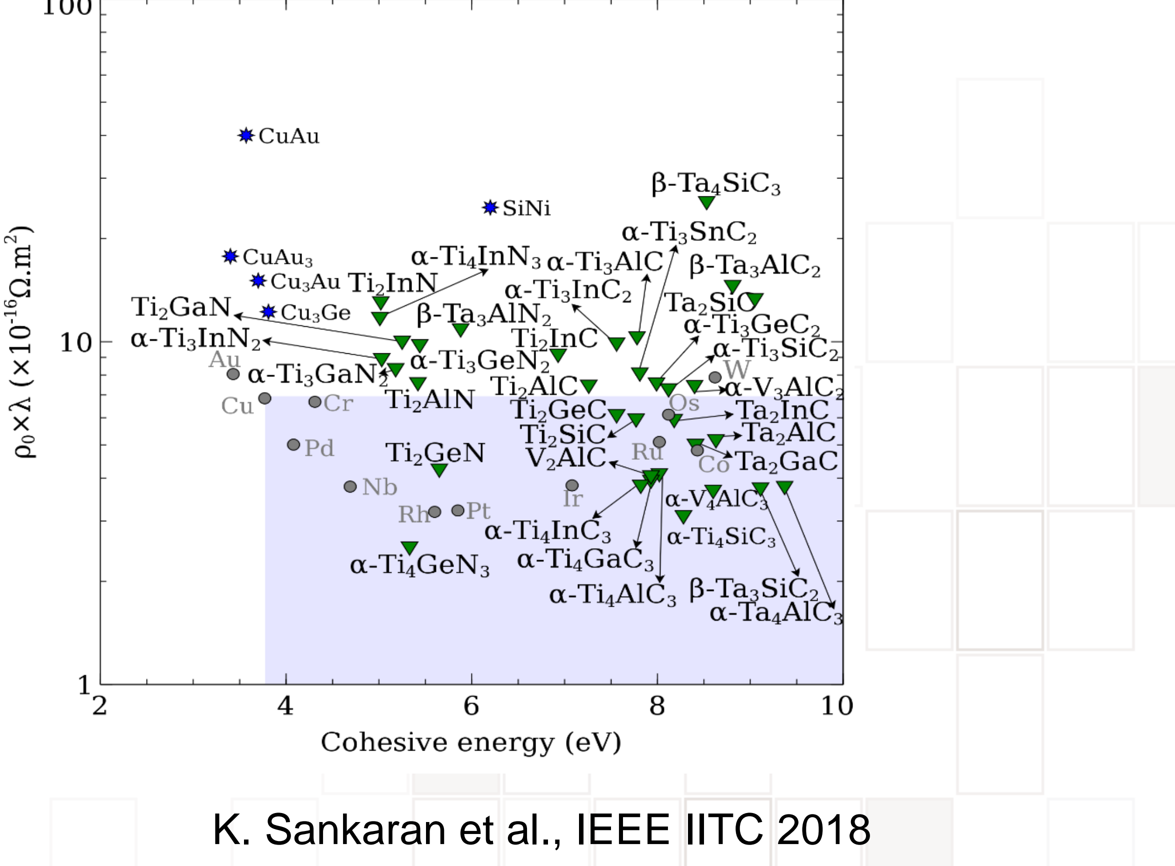



Unleash Innovation

# Interconnect Materials Research

- **Liner and barrier scaling are largely of incremental benefits**
- **Materials exploration beyond elemental options remains important**




K. Sankaran et al., IEEE IITC 2018

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# Interconnect: modeling challenges & opportunities

- Predictive and accurate screening of materials for on-chip electrical interconnect
  - Interconnect disruptive in terms of
    - low-resistance and electro-migration capabilities down to sub 10nm physical dimensions
    - via, via-to-line, and line resistances are pervasive critical performance challenges to address
  - Dielectrics disruptive in terms of low-capacitance / effective lower dielectric constants
- Predictive and accurate screening of ensuing interconnect stack in terms of mechanical integrity under mechanical and/or thermal stress – failure mechanisms and failure modes, heat transport.

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# Building a Functional Virtual Fab from fundamental material properties to system level

- Atomistic simulations: building blocks in predictive TCAD simulations and virtual fab concept

**Performance, power, area, reliability**

Circuit System
Stress, Defects
Device RC...
3D structure
Wafer
Process Steps
...
Process Steps
Design
Layout

## Electrical

**Quantum**
- NEGF
- Schrodinger

**Semi-classical**
- FB KMC

**Classical**
- Drift-Diffusion
- Poisson
- Heat gen / flow

## Physical

**Atomistic**
- MD
- Chemical kinetics

**Semi-classical**
- KMC

**Classical**
- Fluid dynamics
- Thermodynamics
- Mass diffusion

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# Concluding remarks

- Systems with higher levels of performance, functionality, and density continue to require significant energy-efficiency innovations in logic and 3DIC technologies.
- Predictive, accurate and fast TAT modeling from materials to corresponding device-level or interconnect fabric-level remains critical to efficient technology exploration and development.
- Physical representation completeness and self-consistency remain absolute musts to confidently project the expected benefits and/or tradeoffs of novel device, interconnect, and 3DIC concepts relative SOTA capabilities thus contributing to effective screening of exploratory technology options

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