3D Multi-Level-Set Simulation of Bottom Dielectric Isolation Process for Forksheet FETs

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Outline

- Introduction
- In-house Process Simulator Based on Multi-Level-Set Method
- BDI Formation Simulation of FSFET
- Conclusion and Future Work

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- **Introduction**
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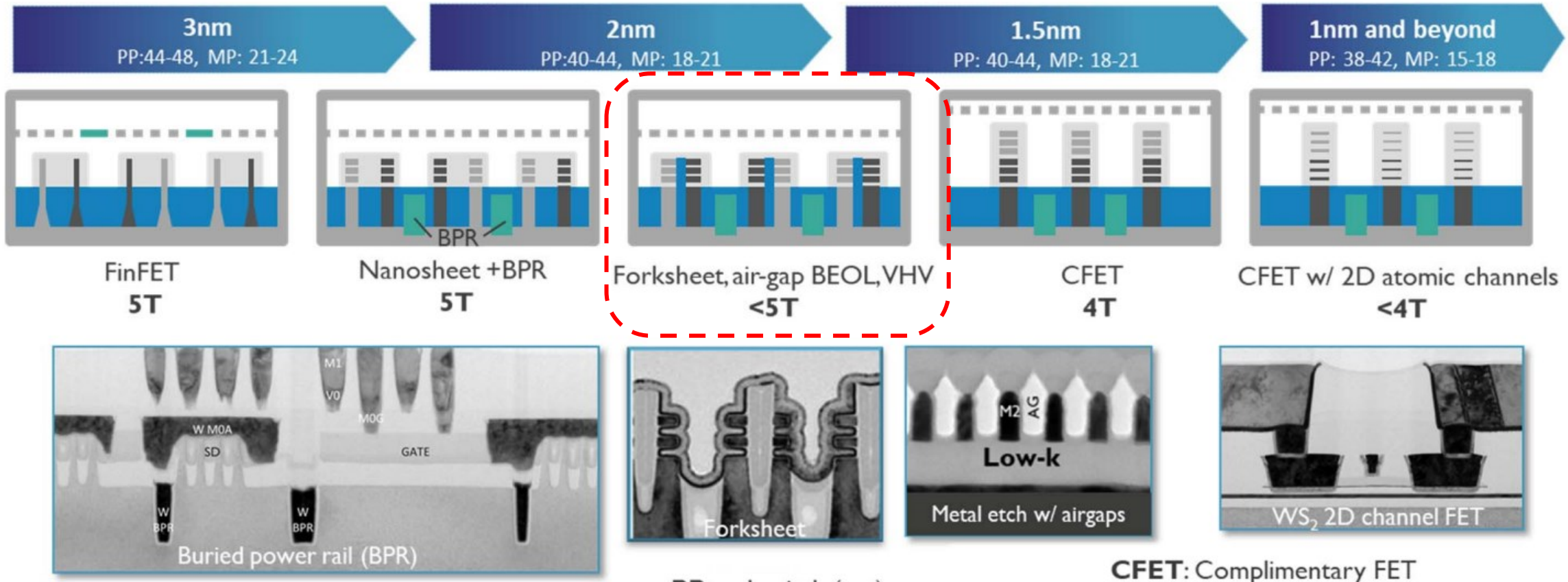
CMOS Technology Scaling Roadmap

- We have moved the era of GAA transistor beyond the FinFET technology
- In the GAA transistor, CMOS scaling continues by improving device architecture



PP: poly pitch (nm)
MP: densest metal pitch (nm)

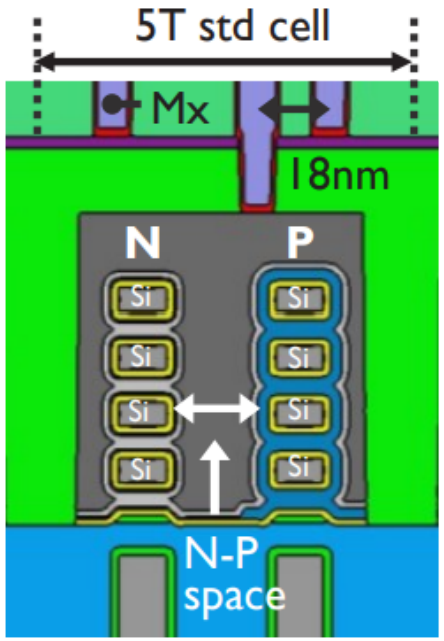
CFET: Complimentary FET
BPR: Buried power rail
VHV:Vertical-Horizontal-Vertical std cell architecture

S. B. Samavedam et al., IEDM 2020

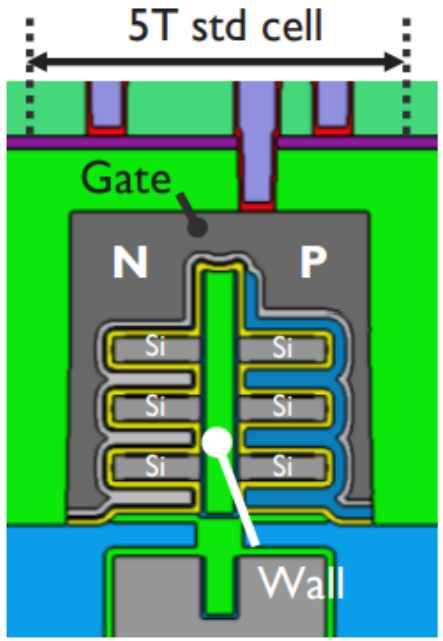
Forksheet FET (FSFET) Transistor

- **FSFET is regarded as a next generation device structure for CMOS scaling owing to their N/P space scaling potential**

Nanosheet FET

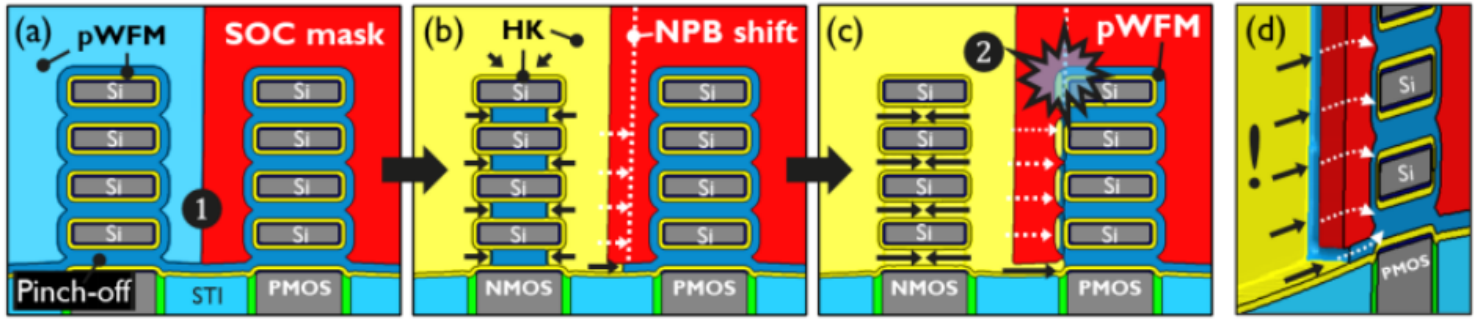


FSFET

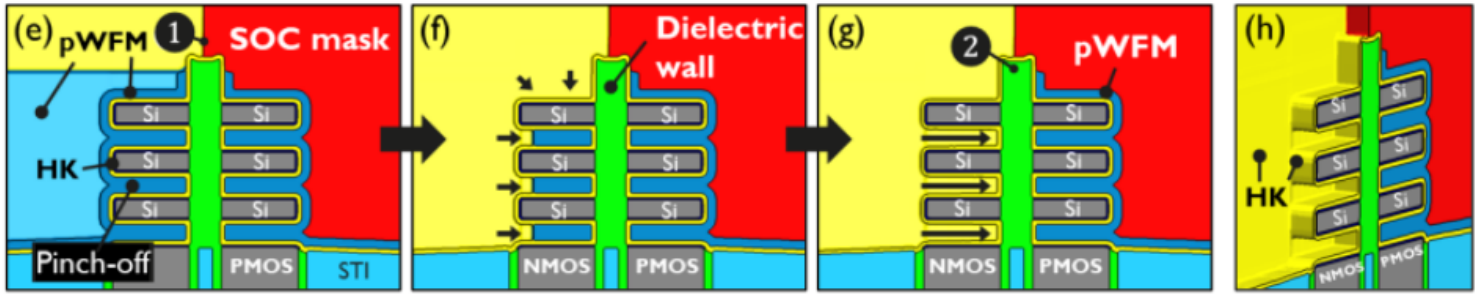


H. Mertens et al., Symposium on VLSI Tech. 2021

Work function metal (WFM) formation for nanosheet FET



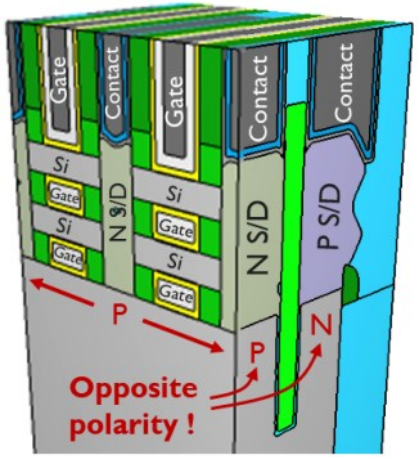
Work function metal (WFM) formation for FSFET



FSFET with Bottom Dielectric Isolation (BDI)

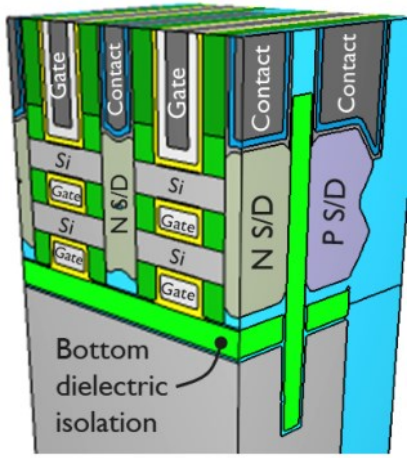
- Challenging substrate doping process is eliminated in FSFET with BDI

FSFET w/o BDI



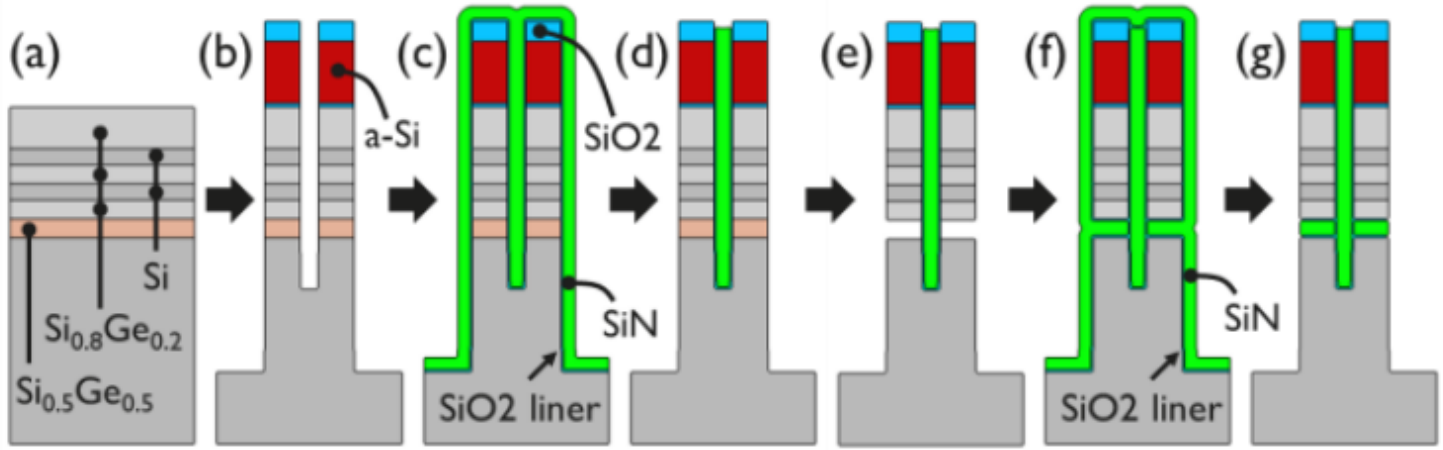
Increase difficulty of substrate doping process

FSFET w/ BDI



Eliminate the doping process

BDI formation process

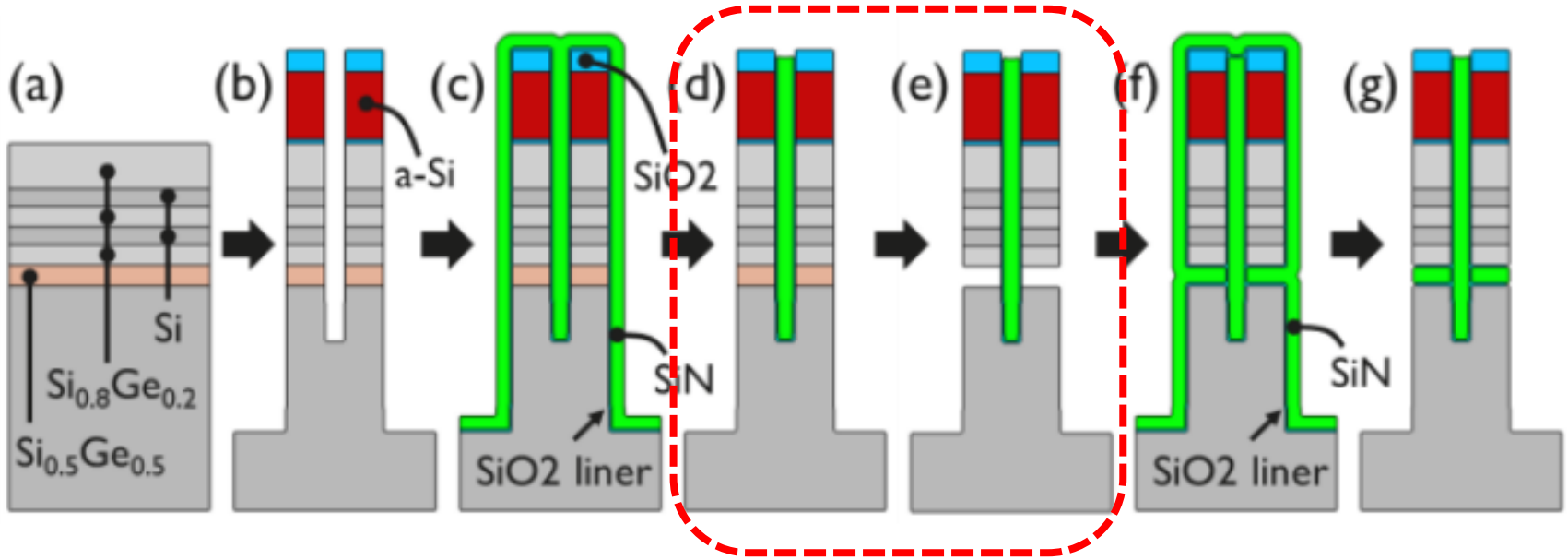


H. Mertens et al., IEDM 2022

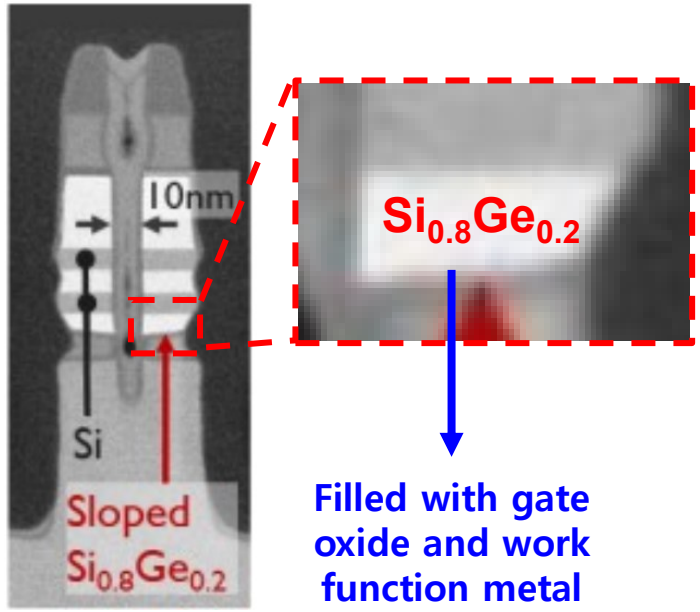
Geometric Problem in BDI Formation Process

- Sloped etch profile of $Si_{0.8}Ge_{0.2}$ is caused due to low selectivity of sacrificial layer ($Si_{0.8}Ge_{0.2}$) to replaced layer ($Si_{0.5}Ge_{0.5}$), which can make problem in later work function metal fill process

BDI formation process



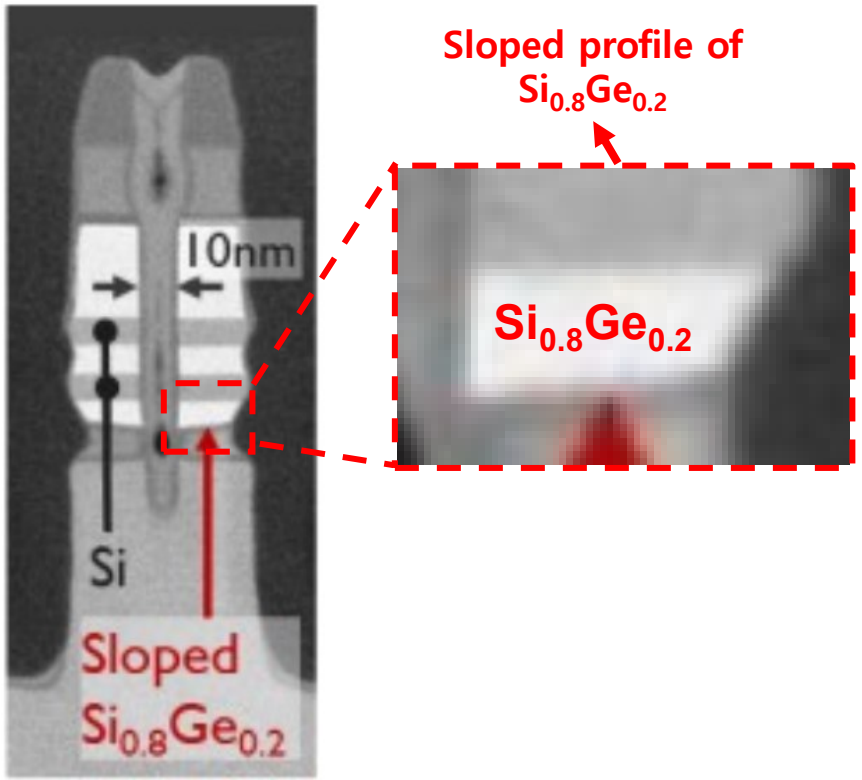
Sloped profile of $Si_{0.8}Ge_{0.2}$ sacrificial layer



Introducing Si Separator for Plat Profile

- The sloped profile can be addressed by introducing the Si separator

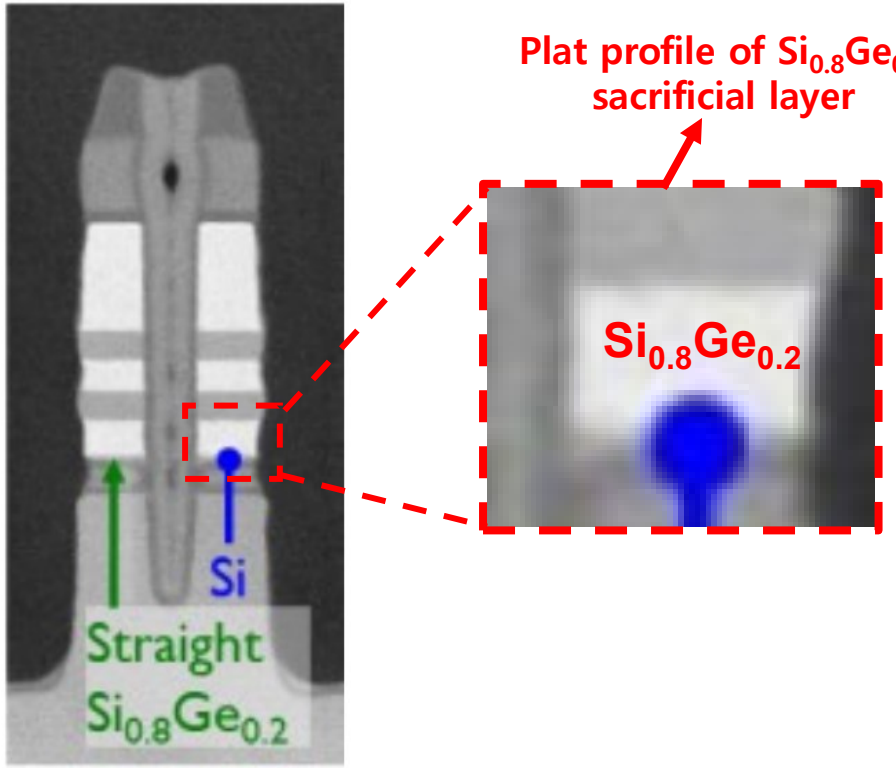
Without Si separator



Sloped profile of $Si_{0.8}Ge_{0.2}$

Adding Si separator

With Si separator



Plat profile of $Si_{0.8}Ge_{0.2}$ sacrificial layer

Numerical investigation is required

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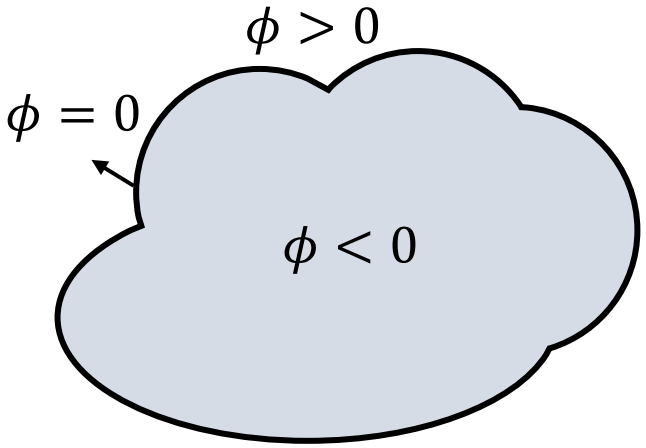
Level-Set Method for Process Simulation

Level-set based implicit boundary representation



Level ϕ is closest distance from boundary

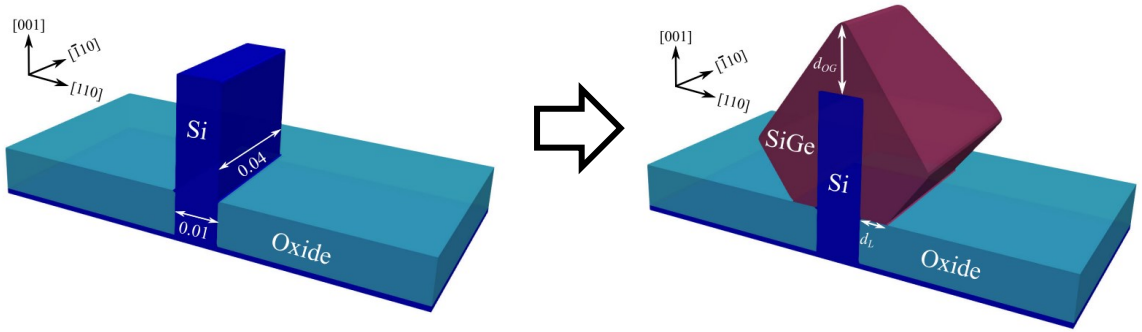
$$\phi = \begin{cases} < 0 & inside\ of\ boundary \\ = 0 & boundary \\ > 0 & outside\ of\ boundary \end{cases}$$

Time evolution of boundary (Hamilton-Jacobi equation)

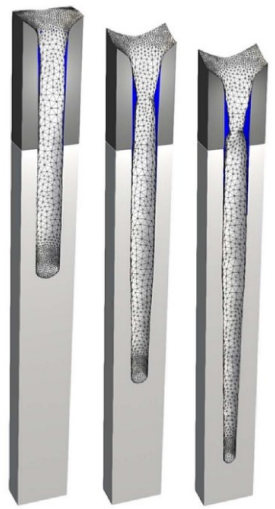
$$\frac{\partial \phi}{\partial t} = V\|\nabla\phi\|$$

ϕ : Level
V : Velocity

Process simulation based on level-set method



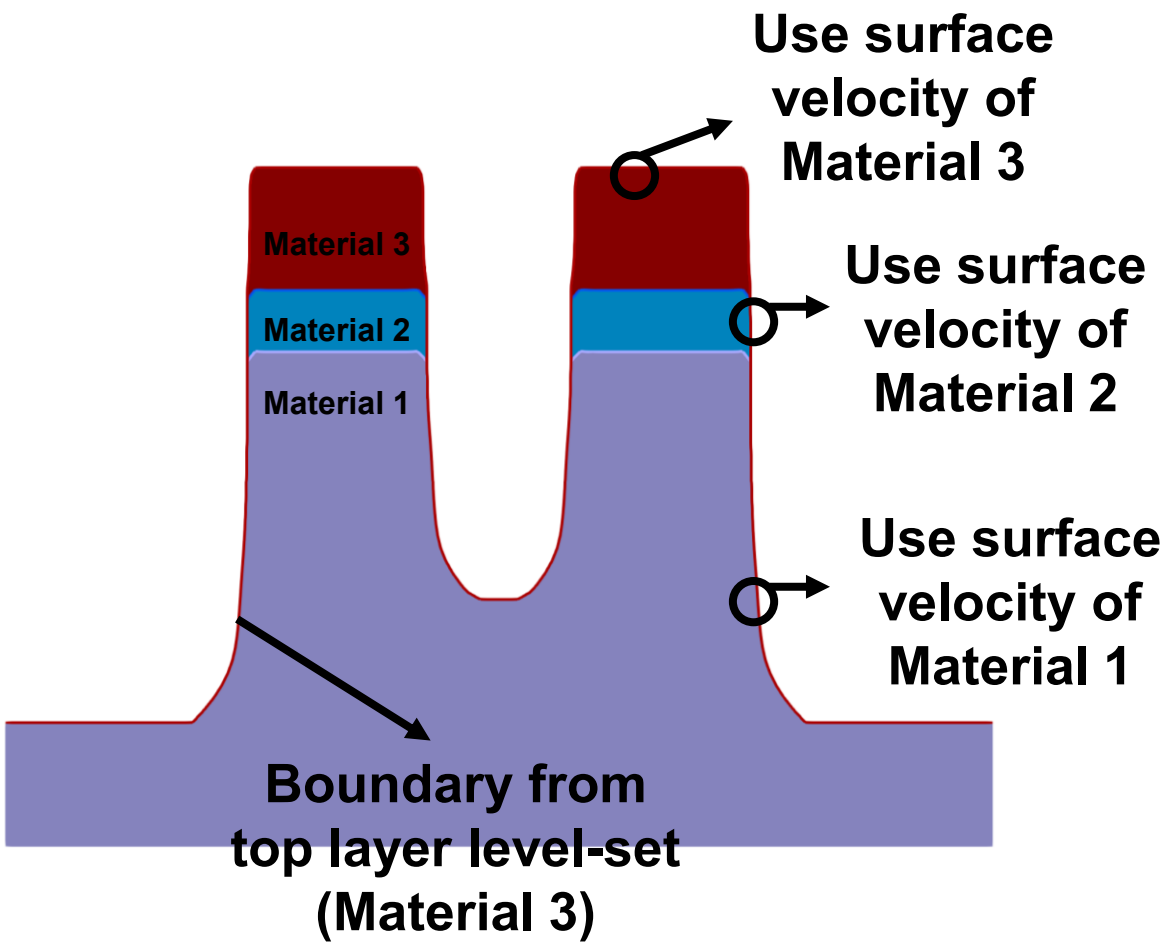
A. Tolifl et al., IEEE Access 2020



Y. G. Yook et al., J. Phys. D: Appl. Phys. 2022

Multi-Level-Set Method

- Boundary motion of multiple material is calculated based on top layer level-set
- Velocity of exposed material is used in time evolution



Updating rule for top layer level-set in time evolution

$$\phi_M^{(t+\Delta t)}(\vec{x}) = \phi_M^{(t)}(\vec{x}) - \sum_{k=1}^{M} \Delta t_k(\vec{x}) \cdot \hat{H}(V_k, \phi_M^{(t)}, \vec{x})$$

$$\Delta t_k(\vec{x}) = \begin{cases} \dfrac{\phi_k^{(t)}(\vec{x}) - \phi_{k-1}^{(t)}(\vec{x})}{\hat{H}(V_k, \phi_M^{(t)}, \vec{x})} \\ \Delta t - \sum_{l=k+1}^{M} \Delta t_l(\vec{x}) \\ 0 \end{cases}$$

ϕ_M: Top layer level-set
ϕ_k: Lower layer level-set

Updating rule for lower layer level-set in time evolution

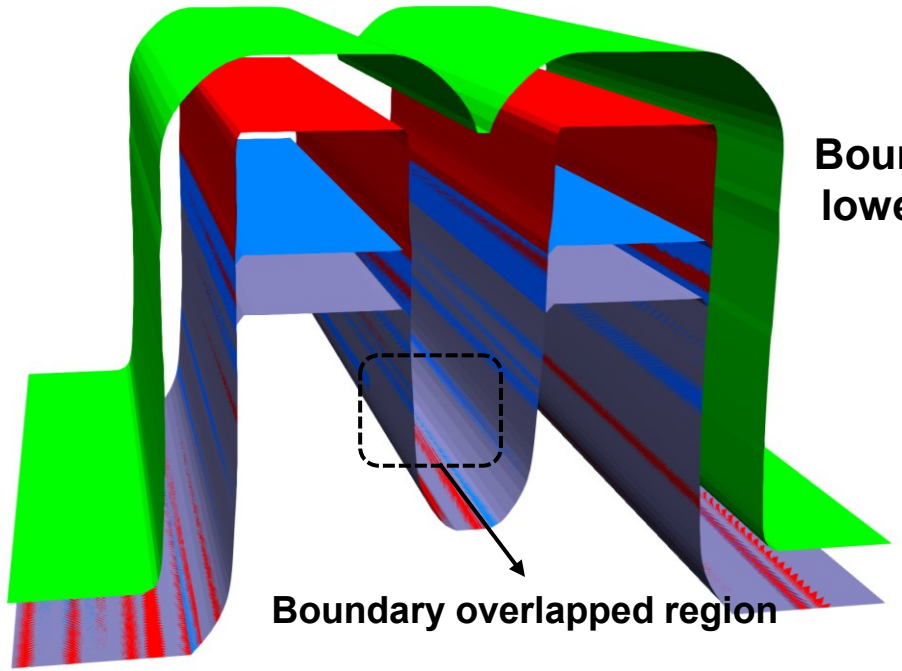
$$\phi_k^{(t+\Delta t)}(\vec{x}) = \max(\phi_M^{(t+\Delta t)}(\vec{x}), \phi_k^{(t)}(\vec{x}))$$

O. Etrl et al., Comput. Phys. Commun. 2009

Closed Boundary Extraction

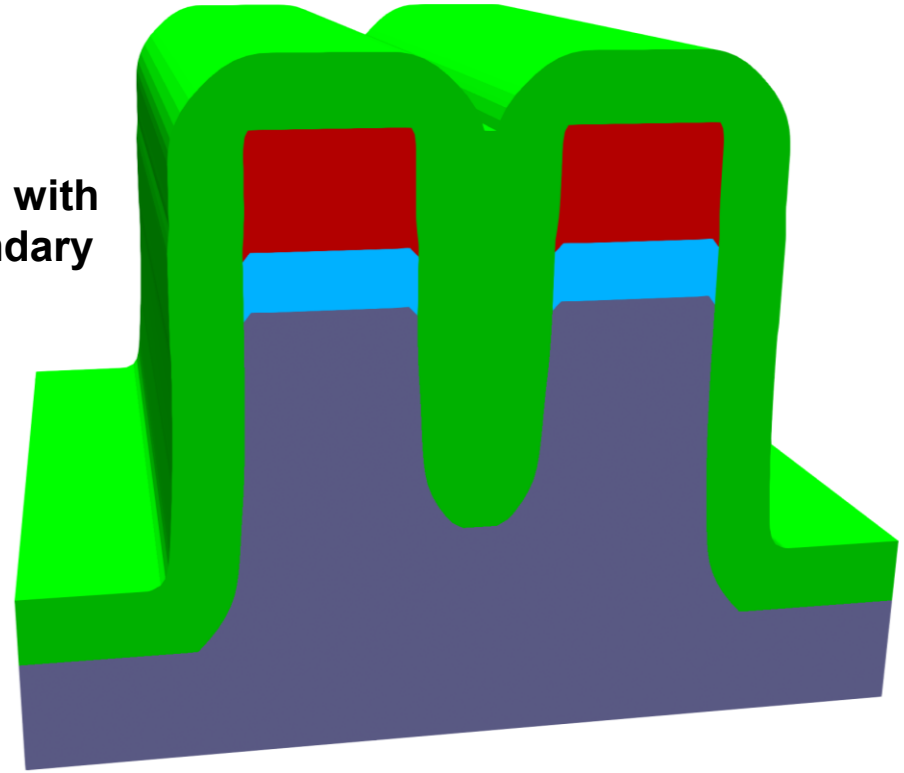
- By extracting lower layer boundary together excluding the boundary of overlapped region, closed boundary is generated

Opened boundary



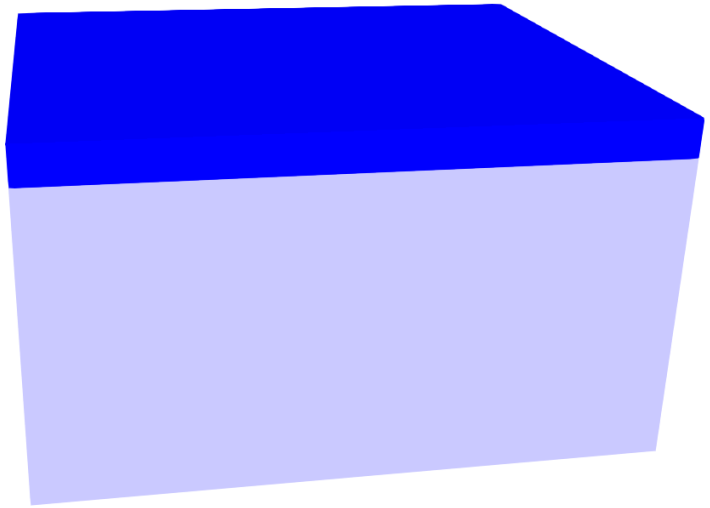
Boundary extraction with lower level-set boundary

Closed boundary

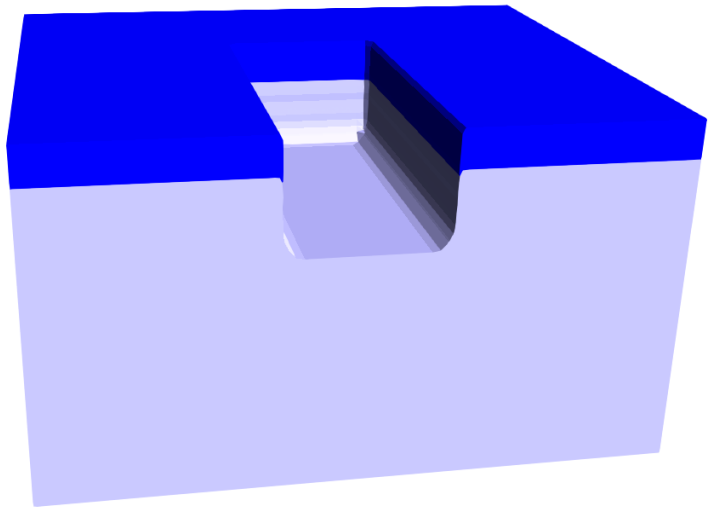


Simple 3D Process Simulation with In-House Tool

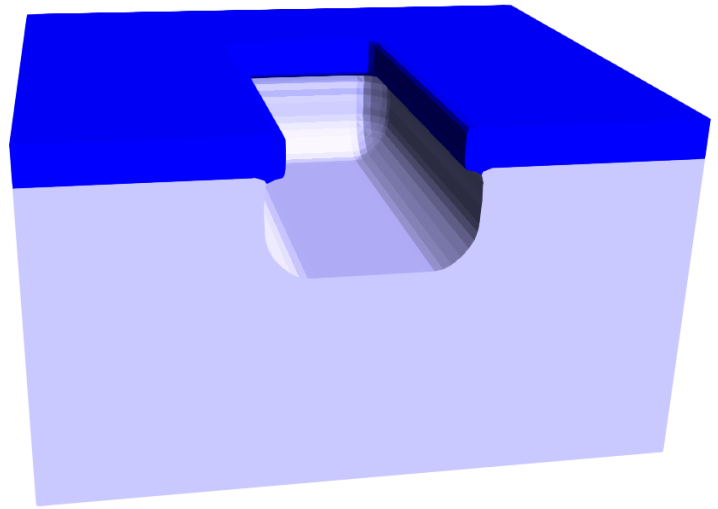
1. Stacked layer



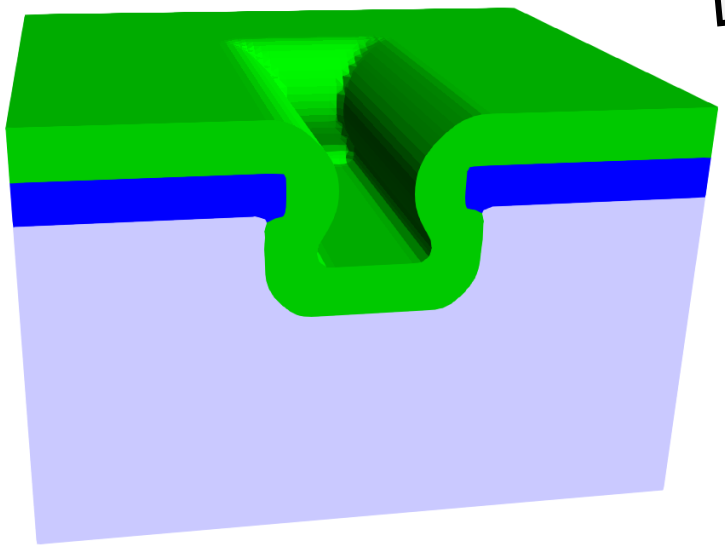
2. Directional etching



3. Selective isotropic etching



4. Conformal deposition



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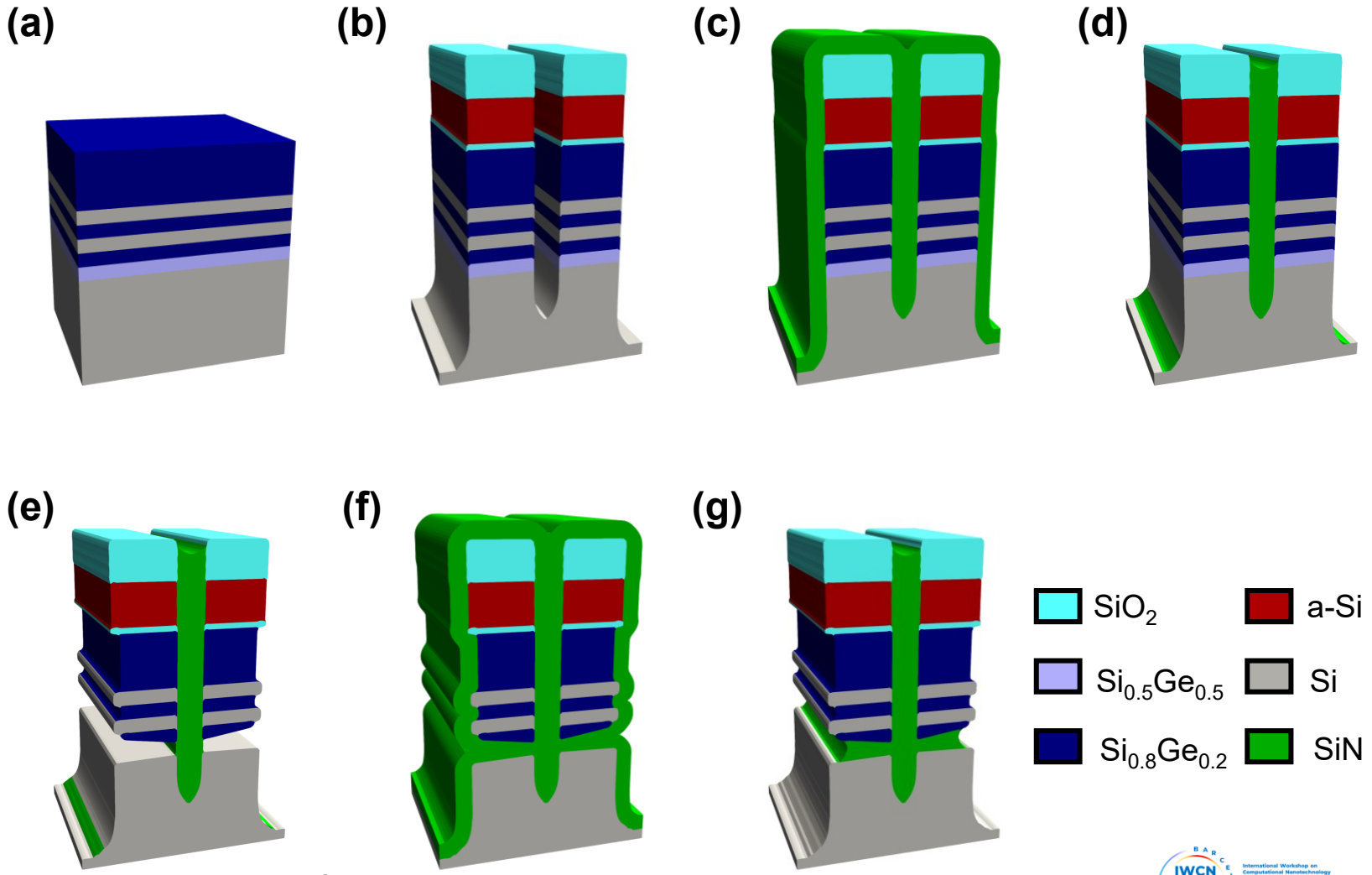
BDI Process Simulation without Si Separator

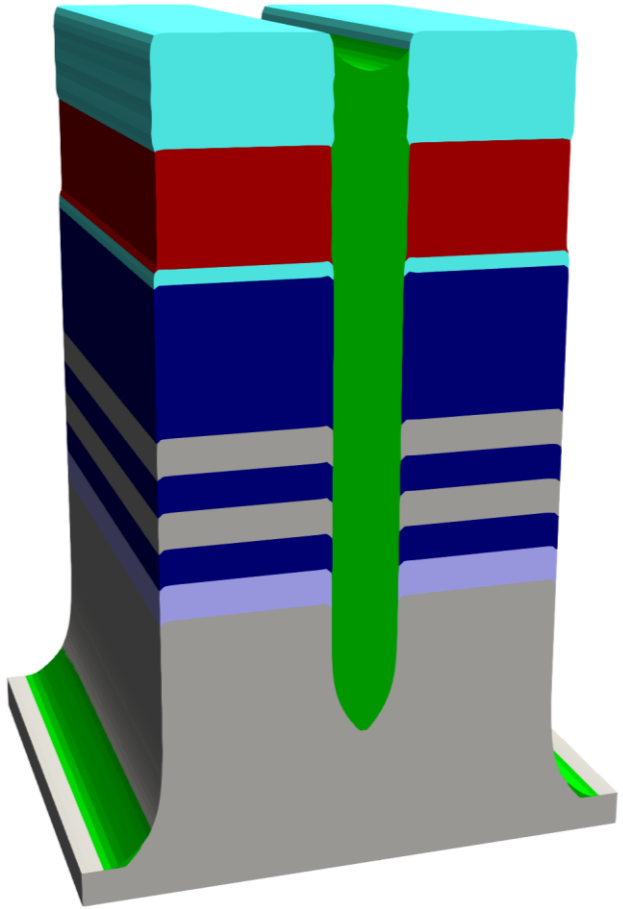
- The process simulation was conducted with in-house process simulator about the case without Si separator

BDI process flow

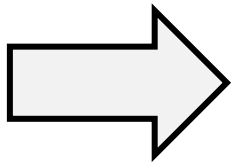
- (a) Si/SiGe multilayer stack
- (b) Fin patterning
- (c) SiN conformal deposition
- (d) SiN isotropic etchback
- (e) $Si_{0.5}Ge_{0.5}$ replaced layer release
- (f) SiN conformal deposition
- (g) SiN isotropic etchback

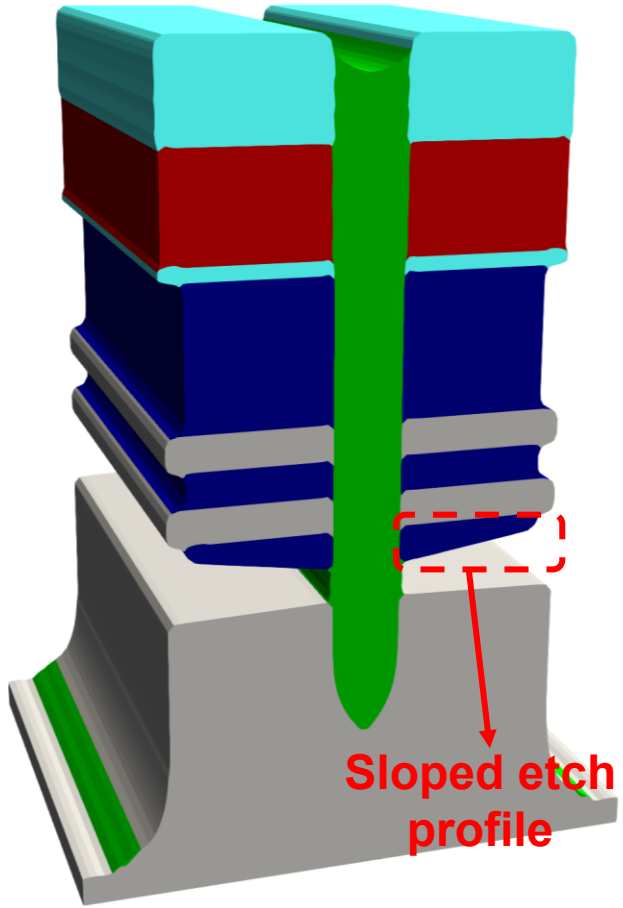


Geometric Problem in $Si_{0.5}Ge_{0.5}$ Release Process



$Si_{0.5}Ge_{0.5}$ replaced layer release





Selectivity

$Si_{0.5}Ge_{0.5}$: $Si_{0.8}Ge_{0.2}$ = 7 : 1

SiO_2 a-Si

$Si_{0.5}Ge_{0.5}$ Si

$Si_{0.8}Ge_{0.2}$ SiN

BDI Process Simulation with Si Separator

- The process simulation was conducted with in-house process simulator about the case with Si separator

BDI process flow

- (a) Si/SiGe multilayer stack
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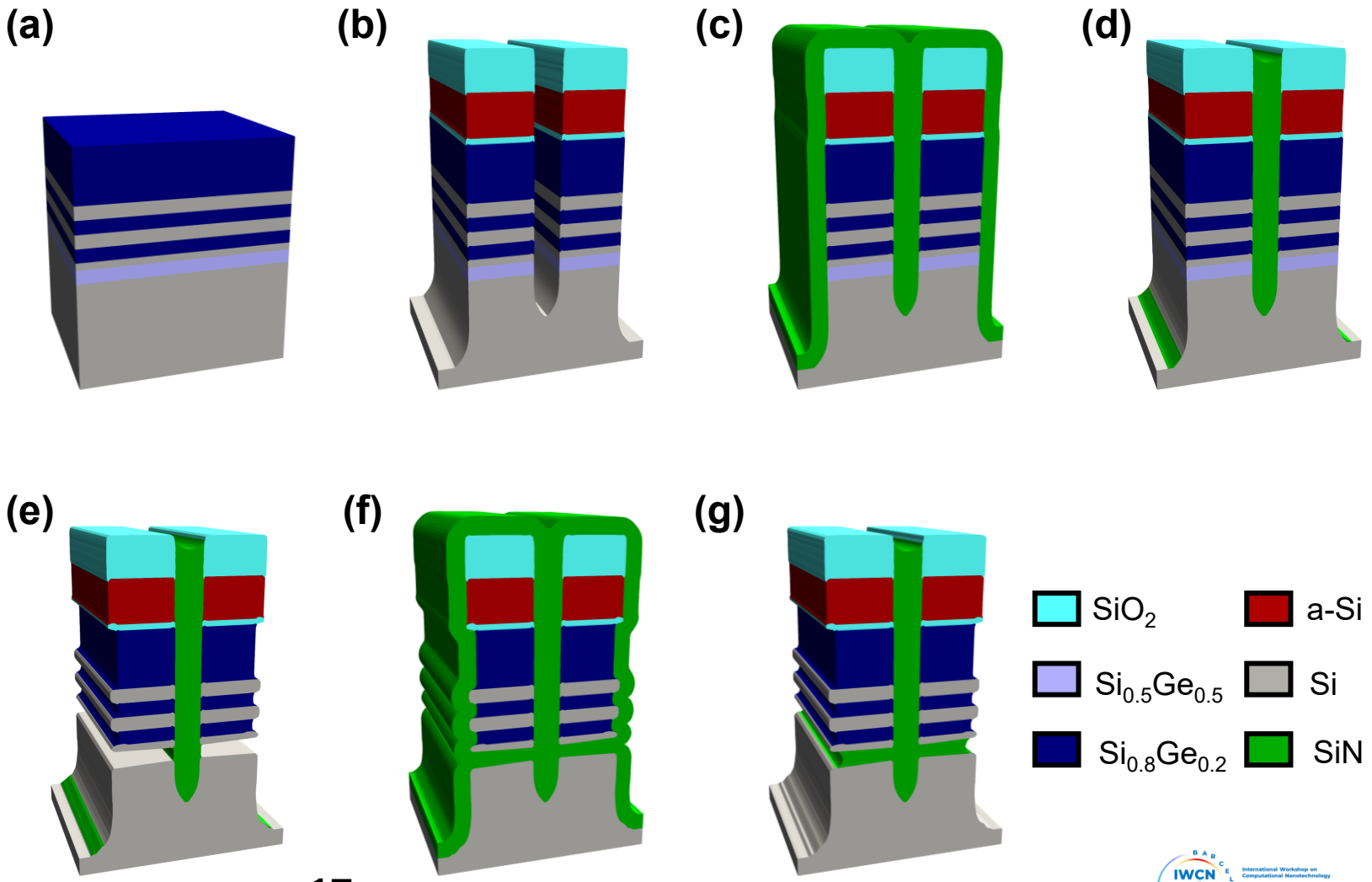
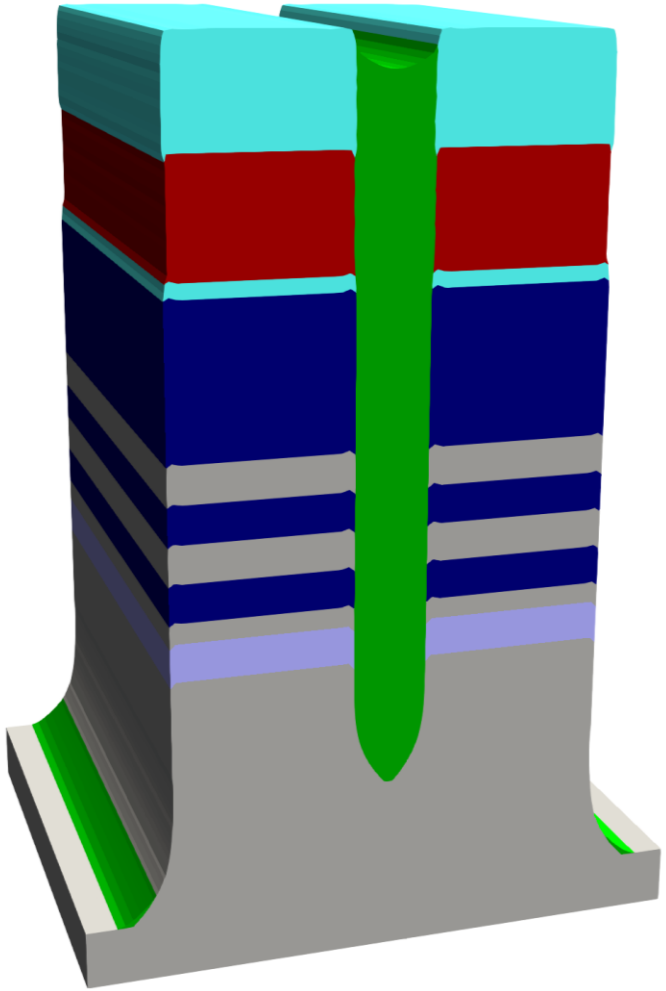
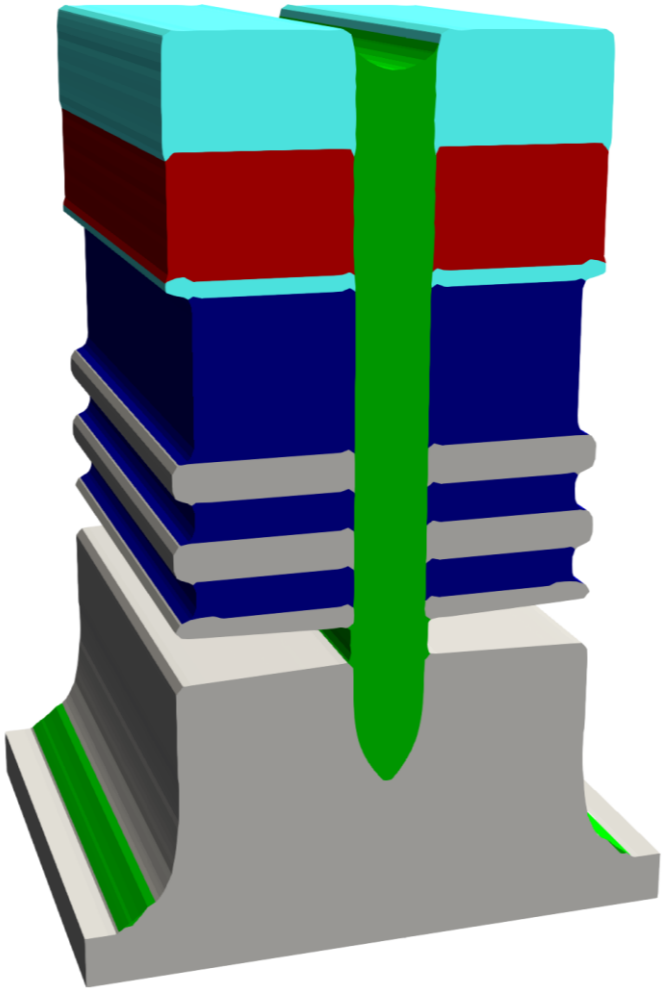


$Si_{0.5}Ge_{0.5}$ Release Process with Si Separator



$Si_{0.5}Ge_{0.5}$ replaced layer release



Selectivity

$Si_{0.5}Ge_{0.5}$: Si = 30 : 1

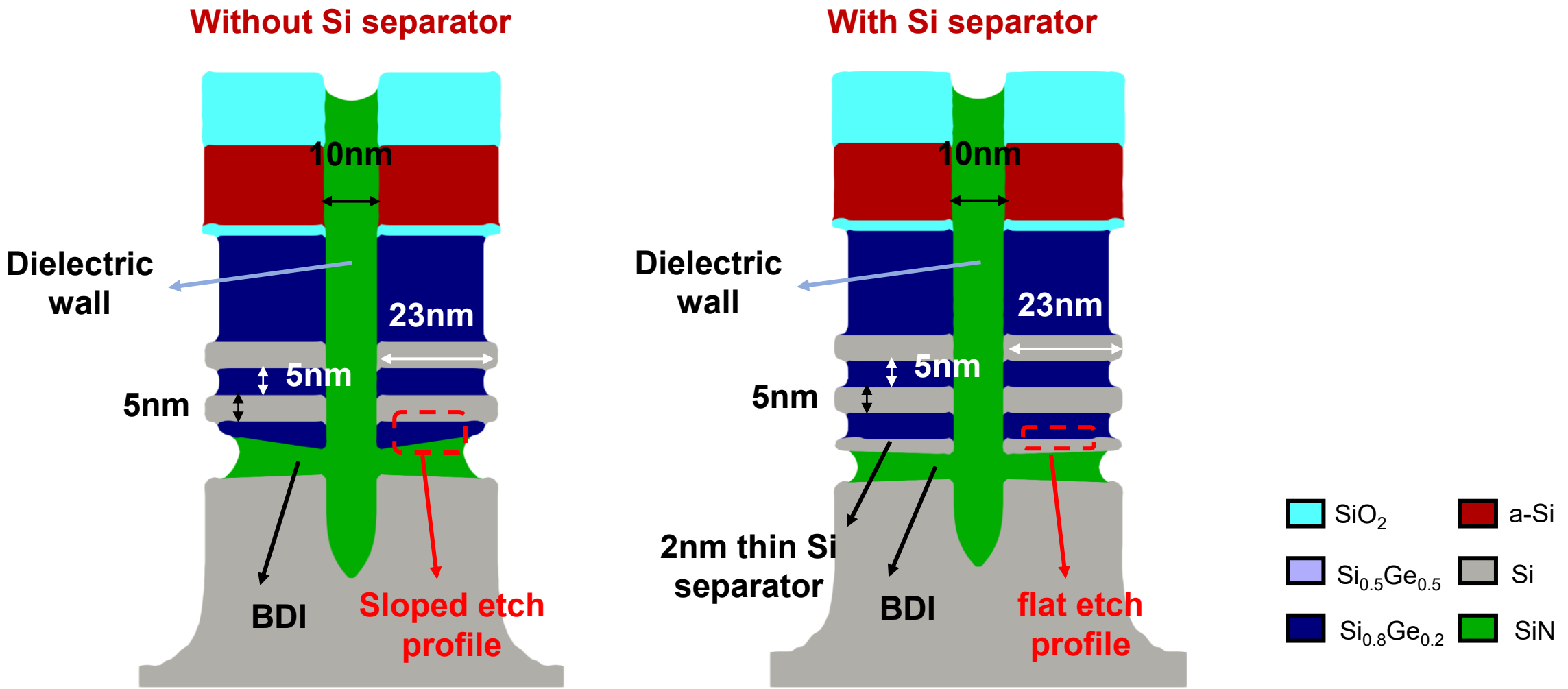
SiO_2 a-Si

$Si_{0.5}Ge_{0.5}$ Si

$Si_{0.8}Ge_{0.2}$ SiN

BDI Process Emulation Result

- The effect of Si separator is numerically investigated with in-house 3D process simulator



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Conclusion and Future Work

Conclusion

- 3D topology simulator based-on level-set method has been developed for the process simulation of GAA logic device
- The effect of Si separator in BDI formation process for FSFET was successfully investigated with the developed in-house process simulator

Future work

- Entire process simulation of BDI FSFET will be conducted with developed in-house simulator
- Device simulation of generated device will be conducted by integrating the in-house process simulator with our in-house TCAD device simulator “G-Device”

Thank you

Acknowledgement

- **Financial support**
  - National Research Foundation of Korea (NRF)
    - NRF-2020M3H4A3081800