Process Simulation in Micro- and Nano-Electronics

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Outline

- Process TCAD for design technology co-optimization (DTCO)

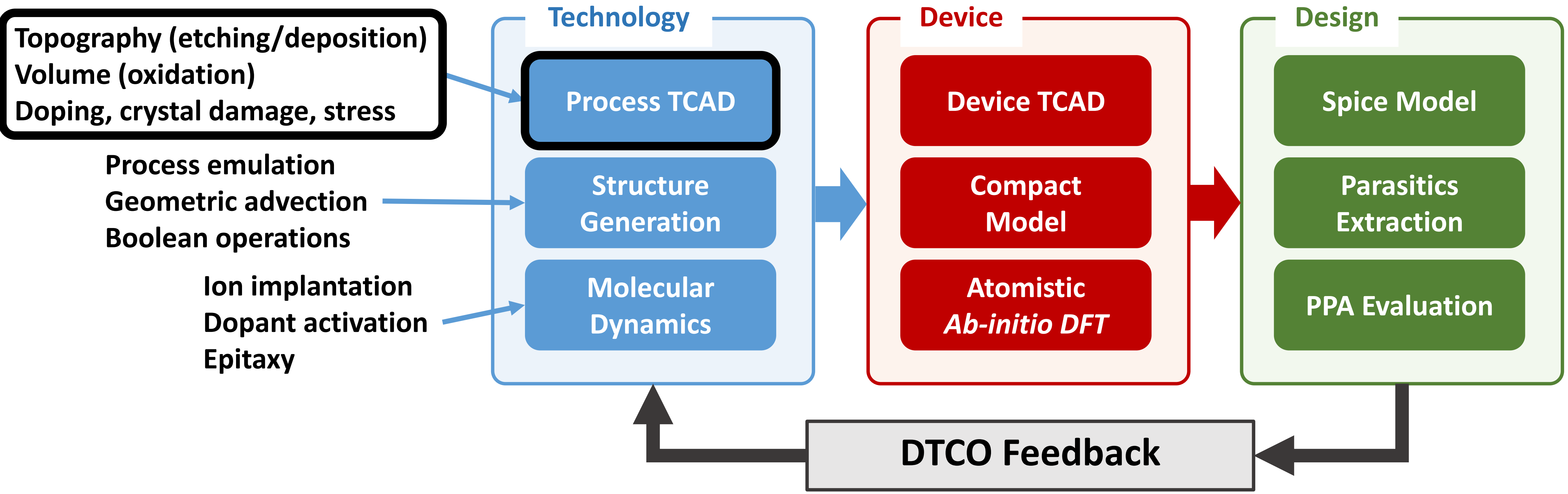
- Combined topography and volume simulations
  - ViennaPS (Process Simulator) framework
  - Ion implant damage during plasma etching
  - By-product redeposition on SiO_2 during Si_3N_4 etching of 3D NAND stacks

- Fast structure generation for DTCO
  - Compact model for SF_6/O_2 plasma etching
  - DTCO study of the circuit-level impact of air spacer fabrication

- Multi-scale problems
  - Al implantation in SiC with Molecular Dynamics

Introduction – What is DTCO?

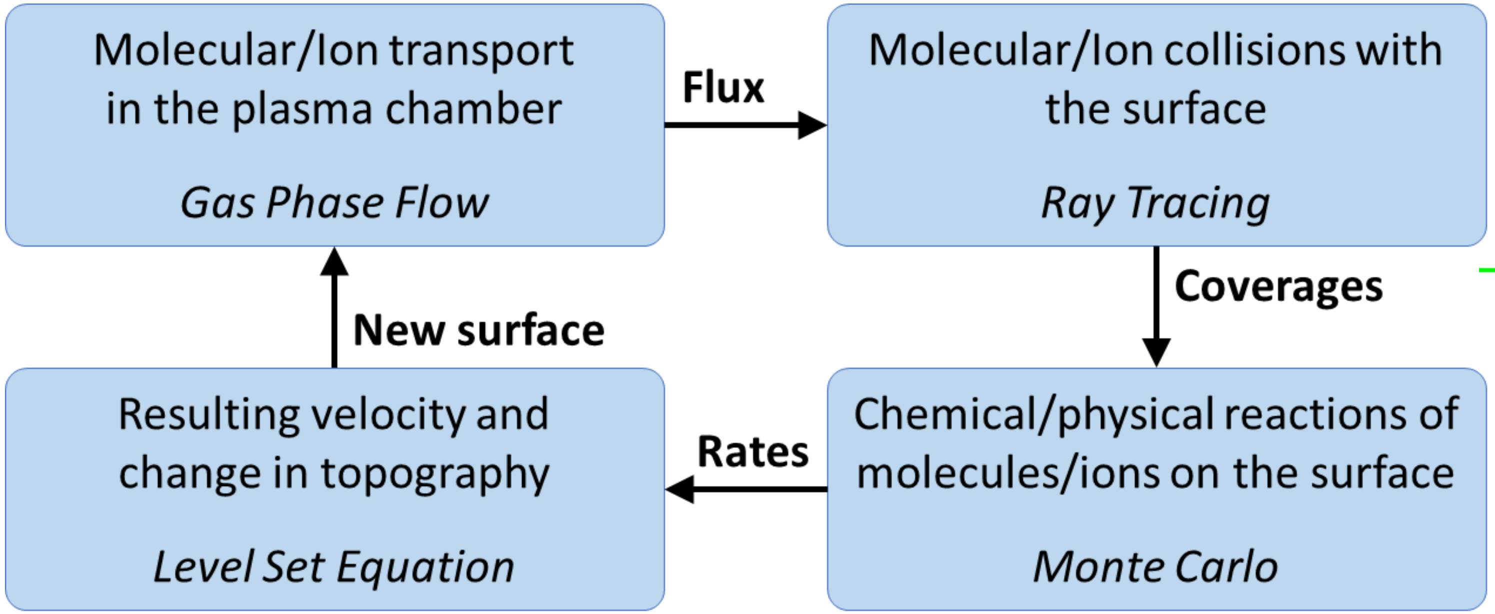
- In the TCAD community, we like to think of it as a flow with a feedback loop

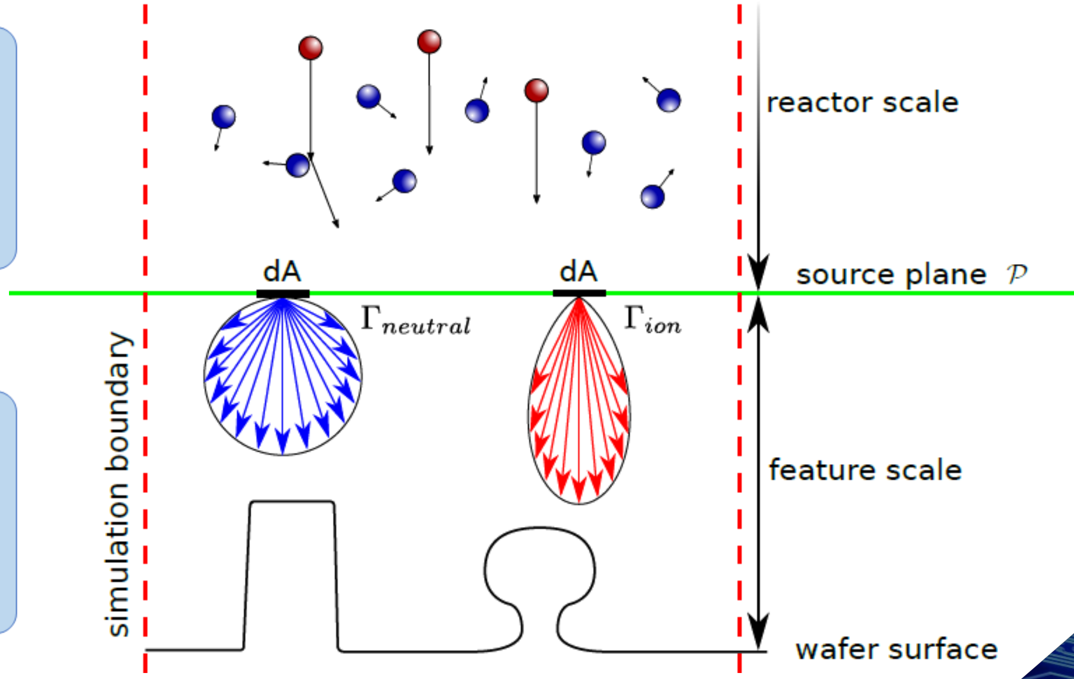


Process TCAD – Physical Modeling

Physical simulations using Process TCAD:

- Physically highly accurate
- Can be used to adjust or calibrate processes
- Requires significant time and is computationally expensive
- May require complex mesh conversions for Device TCAD

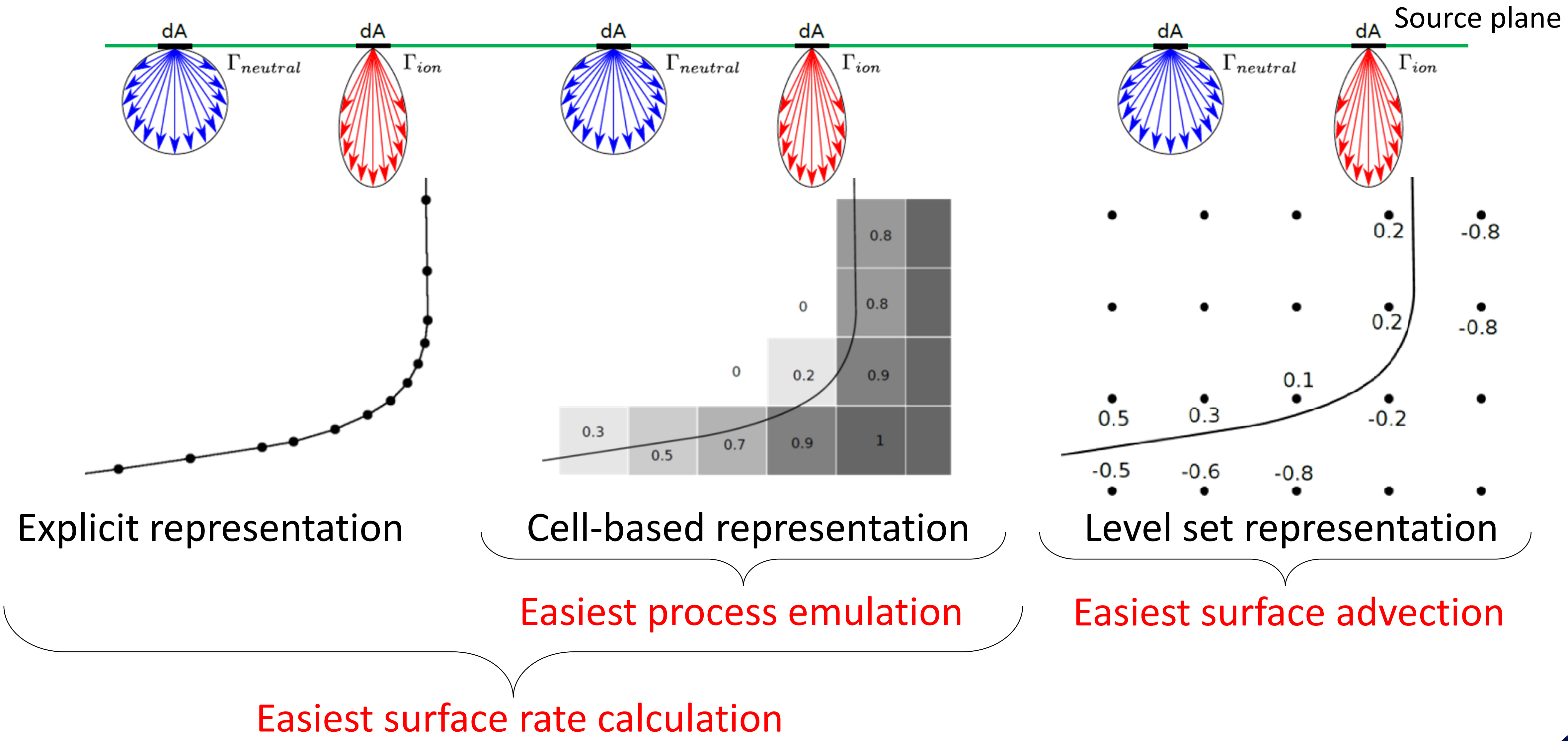




X. Klemenschits et al., Micromachines 9(12), 2018
J. Bobinac et al., Micromachines 14(3), 2023

Process TCAD – Physical Modeling

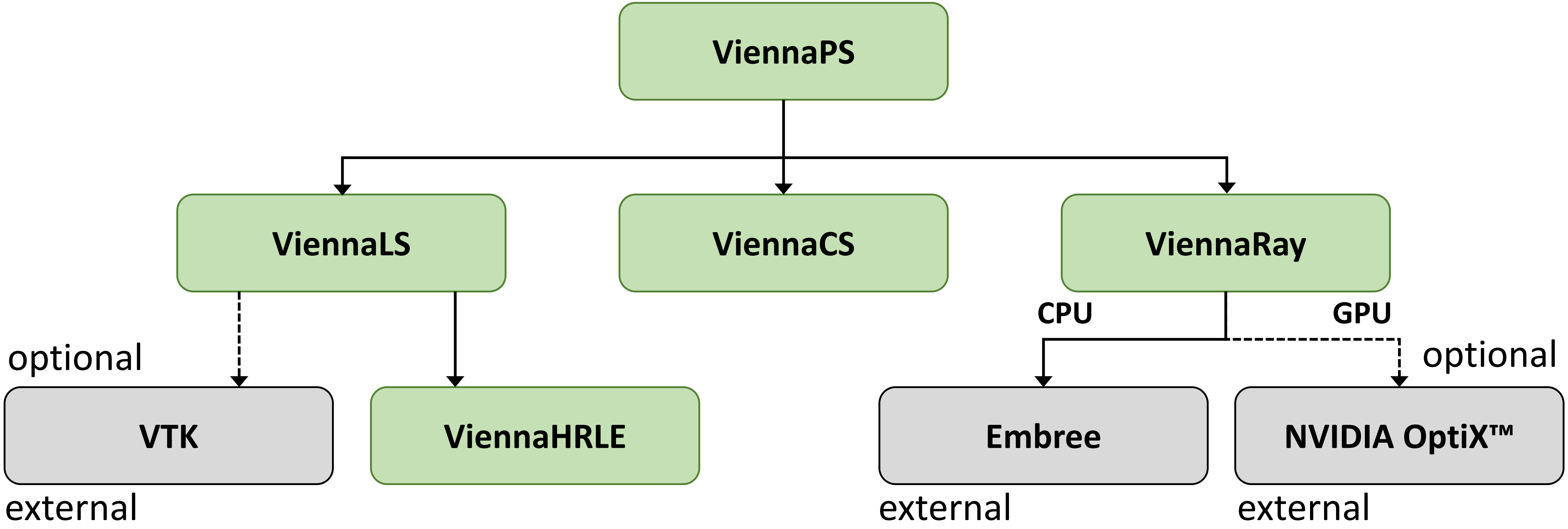
Surface representation



Process TCAD – ViennaPS Framework

The Vienna Process Simulator (ViennaPS)

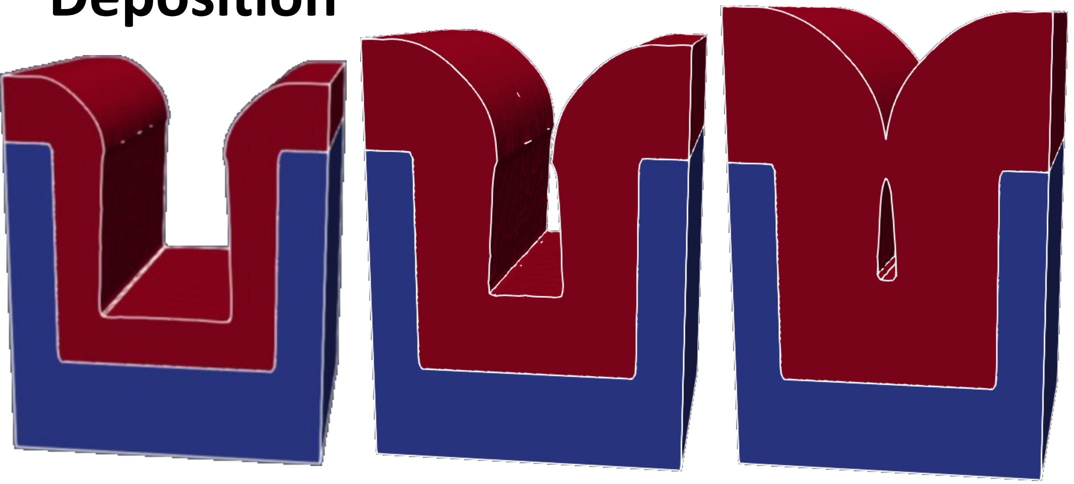
- Process (physical) simulation and (geometric) emulation
- Simultaneous surface (ViennaLS) and volume representation (ViennaCS)
- Initial geometry can be drawn or imported (GDSII, VTK, etc.)



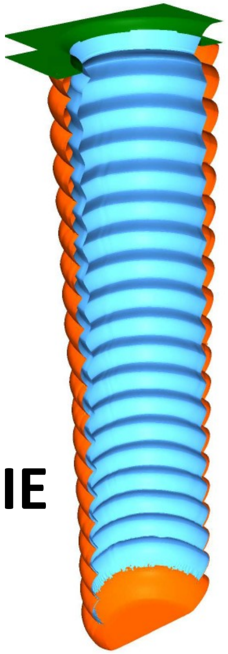
ViennaPS: https://github.com/ViennaTools/ViennaPS

Process TCAD – Physical Modeling with ViennaPS

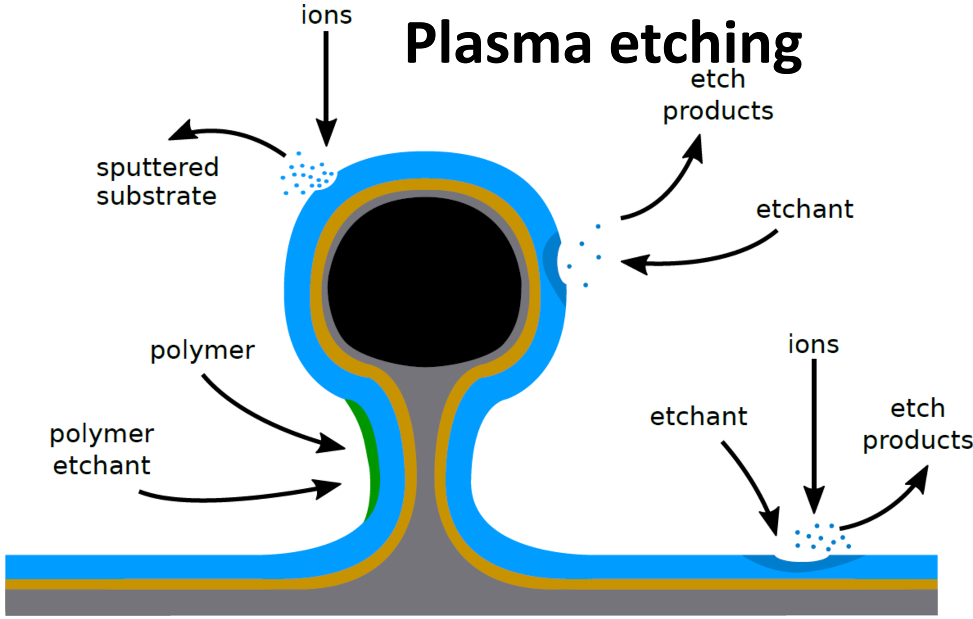
Deposition



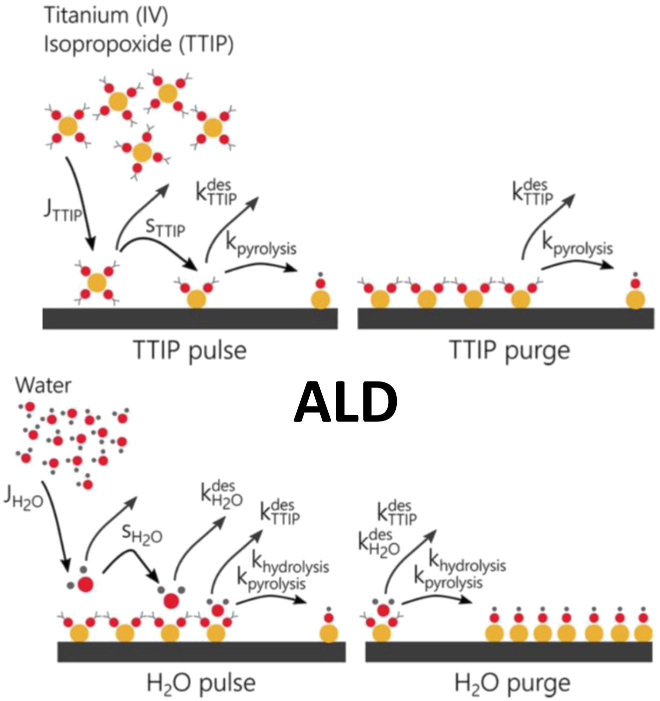
DRIE

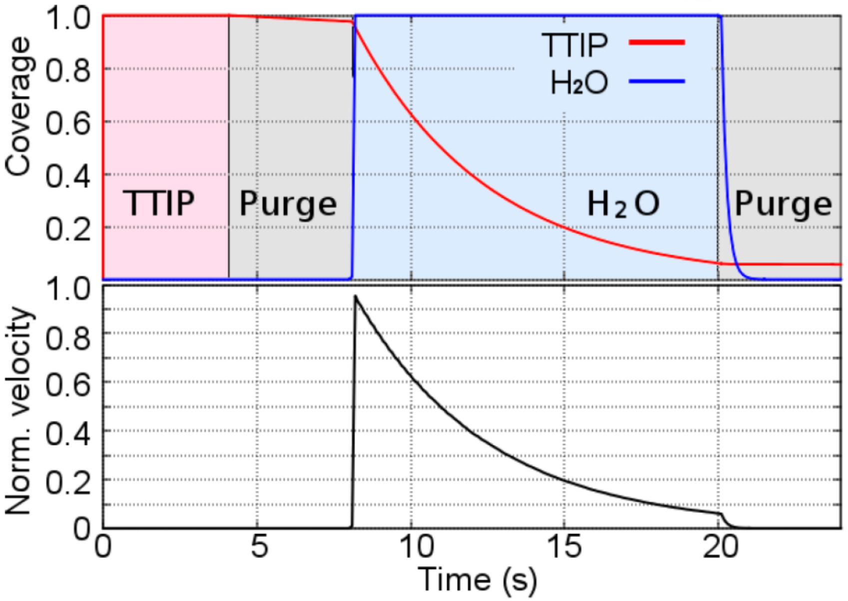


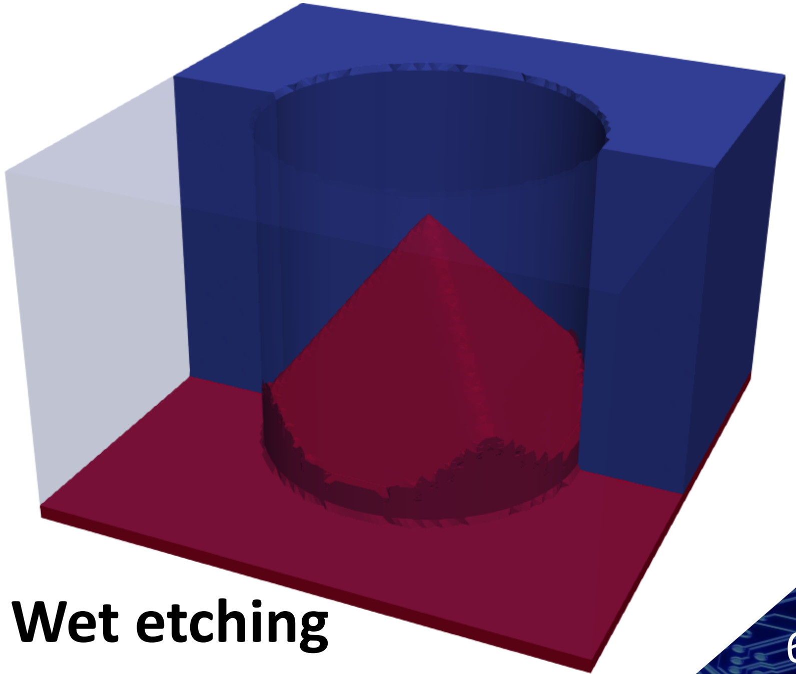
Plasma etching



ALD



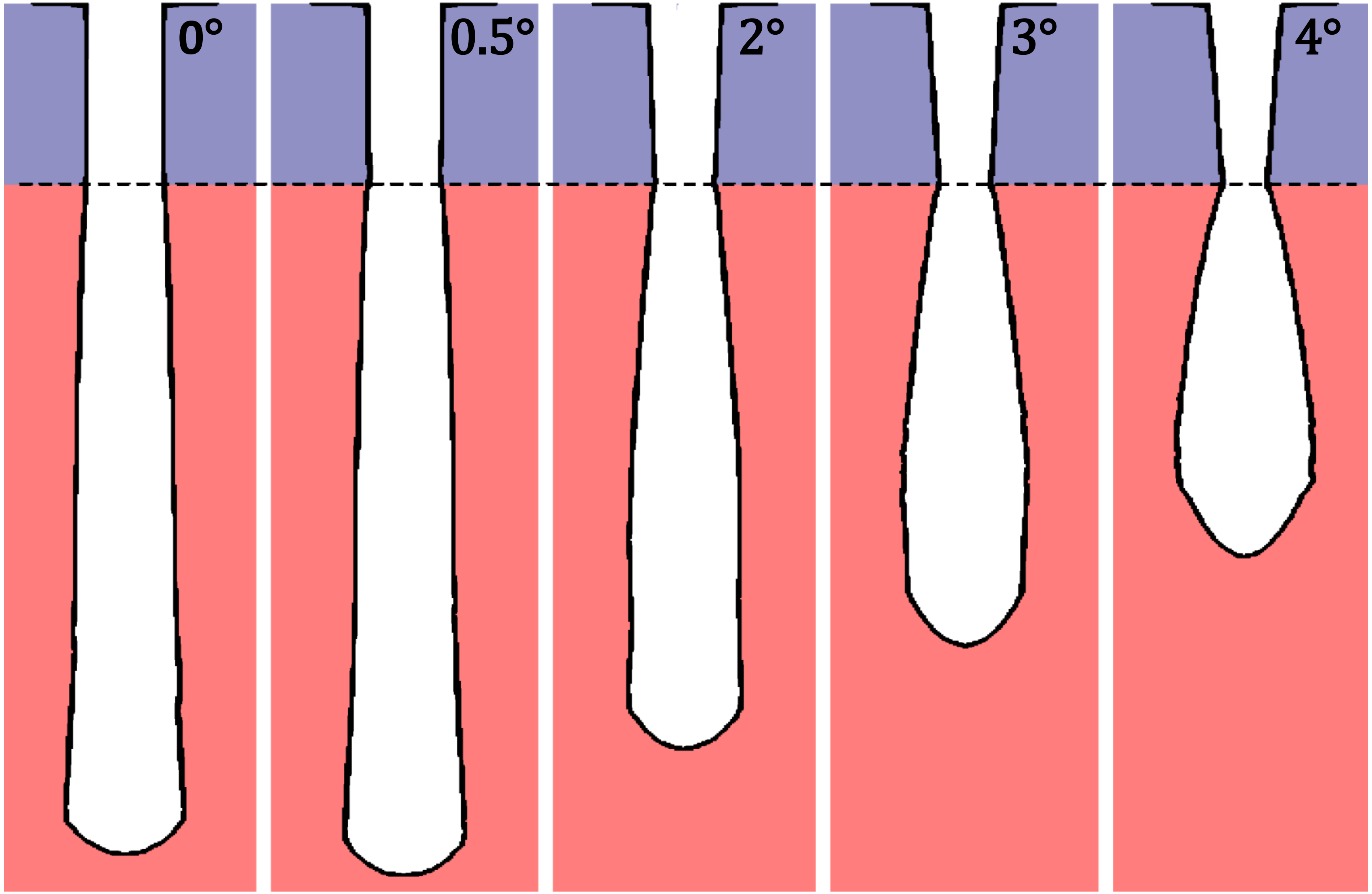


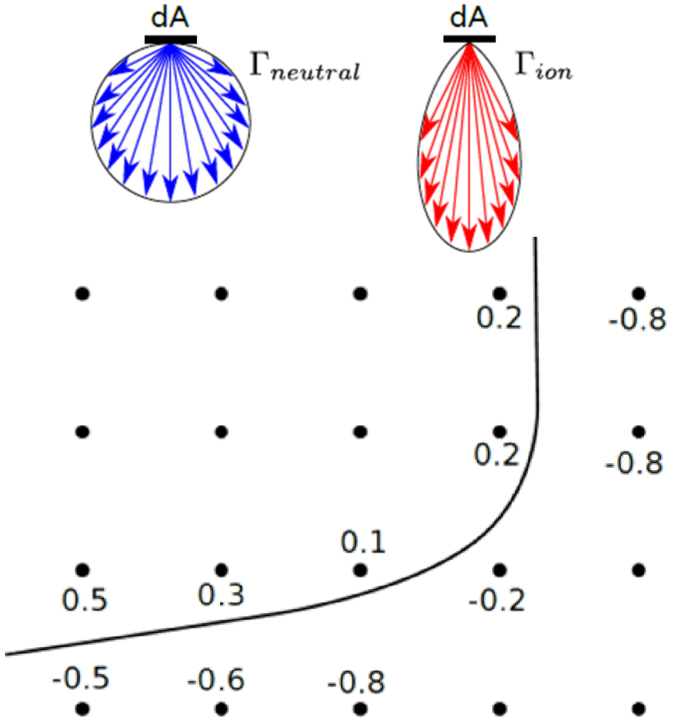


Wet etching

Process TCAD – Physical Modeling with ViennaPS

- Level Set for topography simulation – Etching



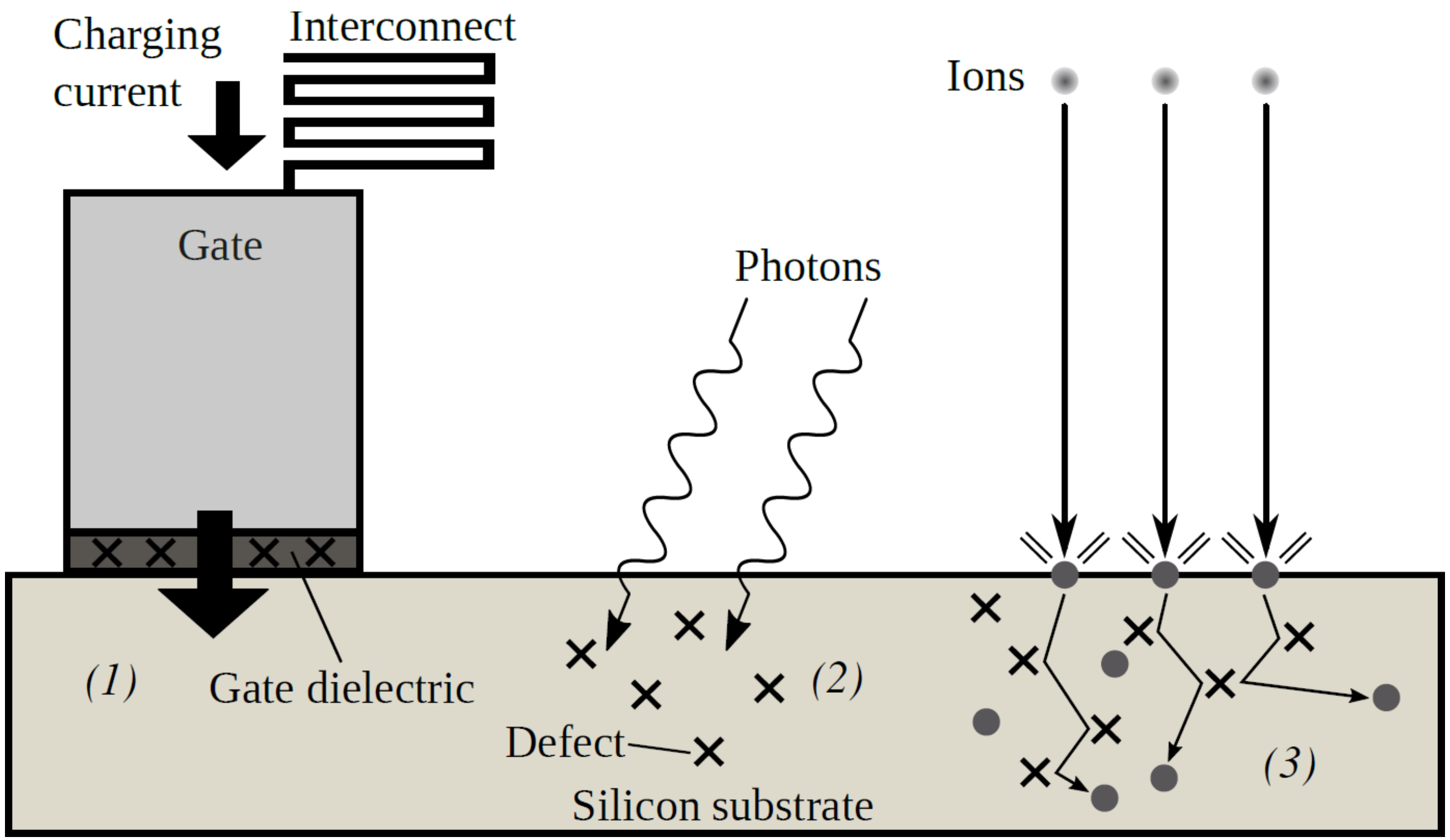


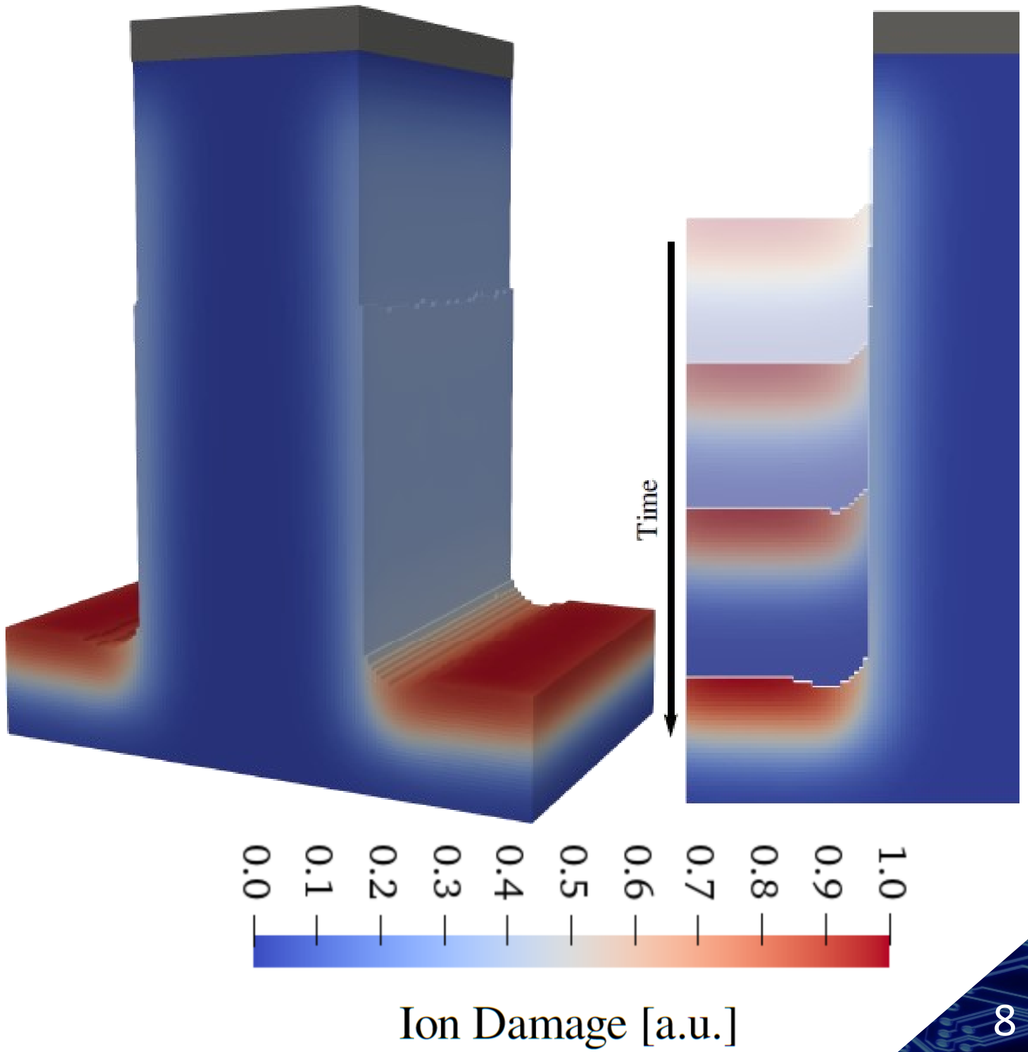
Level set representation

J. Bobinac et al., Micromachines 14(3), 2023

Process TCAD – Combined Topography and Volume Processes

- Tracking ion implant damage during reactive ion etching combines Monte Carlo ray tracing and Binary Collision Approximation



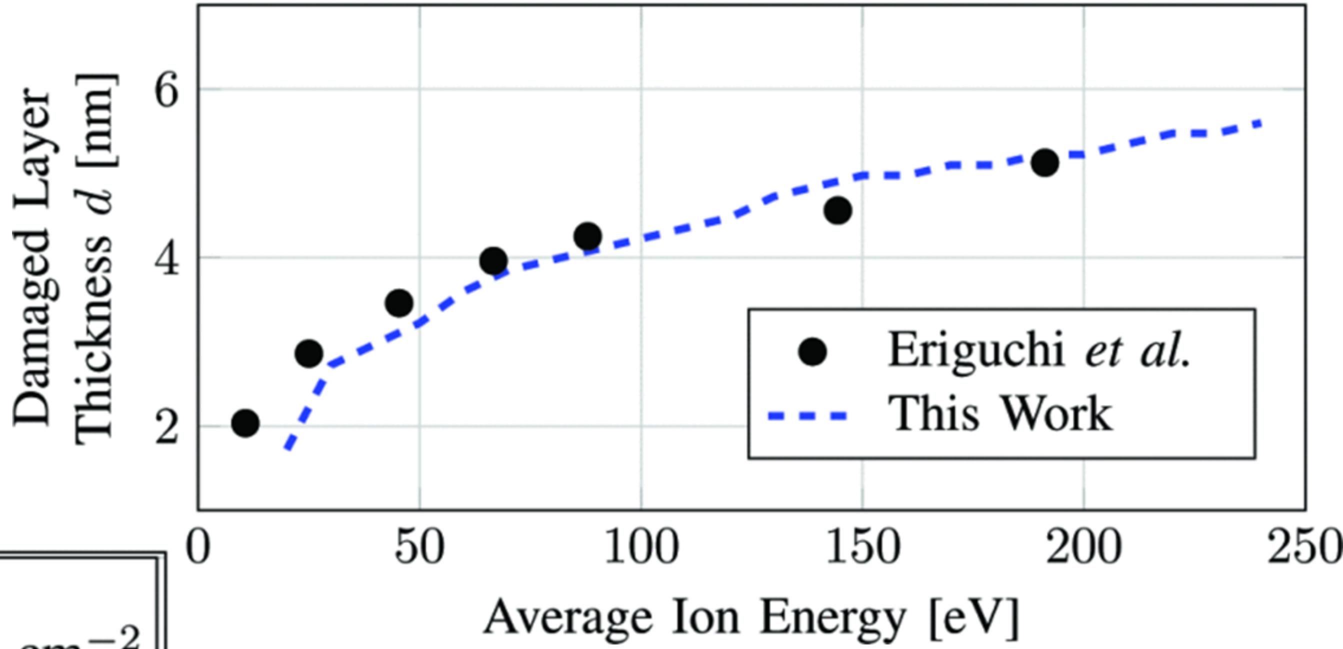


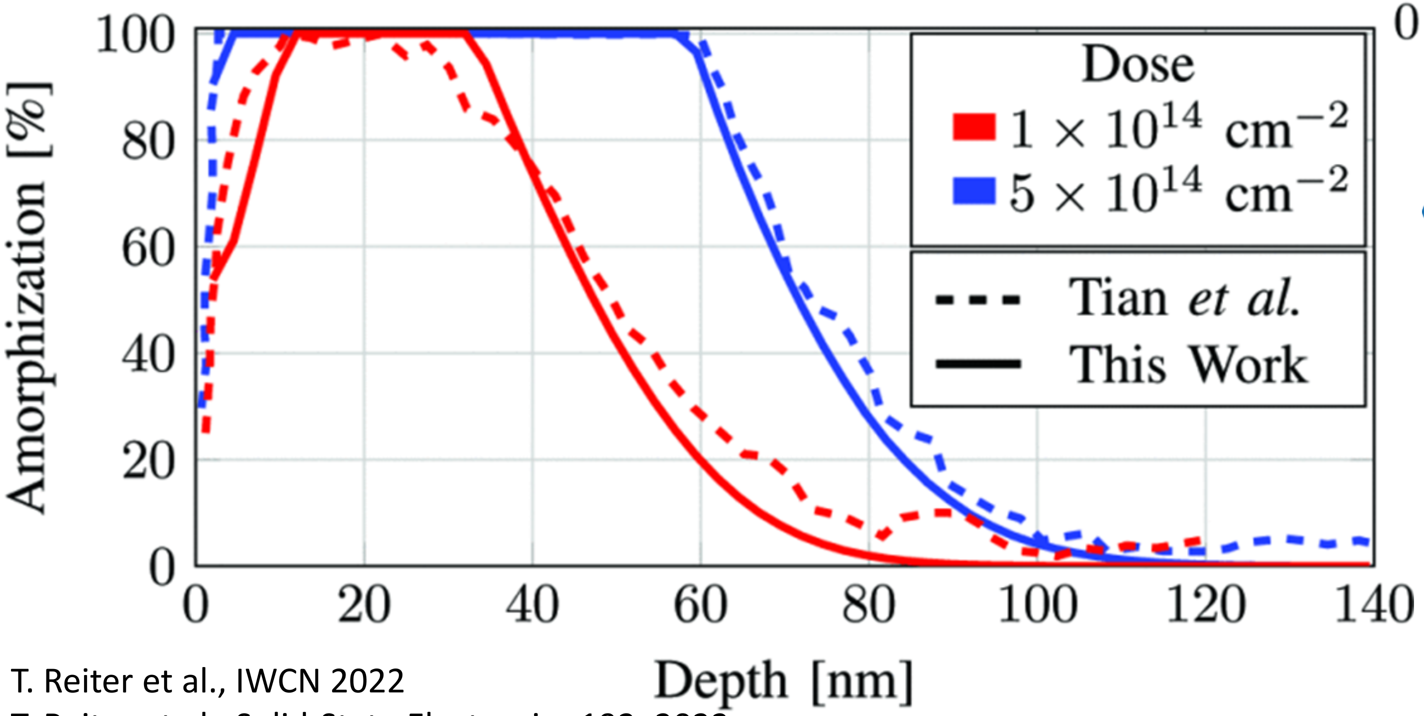
T. Reiter et al., IWCN 2022
T. Reiter et al., Solid-State Electronics 192, 2022

Process TCAD – Tracking Ion Implant Damage

- Impact of average ion energies on the thickness of the damaged (non-crystalline) layer compared to experimental data by Eriguchi et al.

K. Eriguchi et al., Japanese Journal of Applied Physics 49, 2010





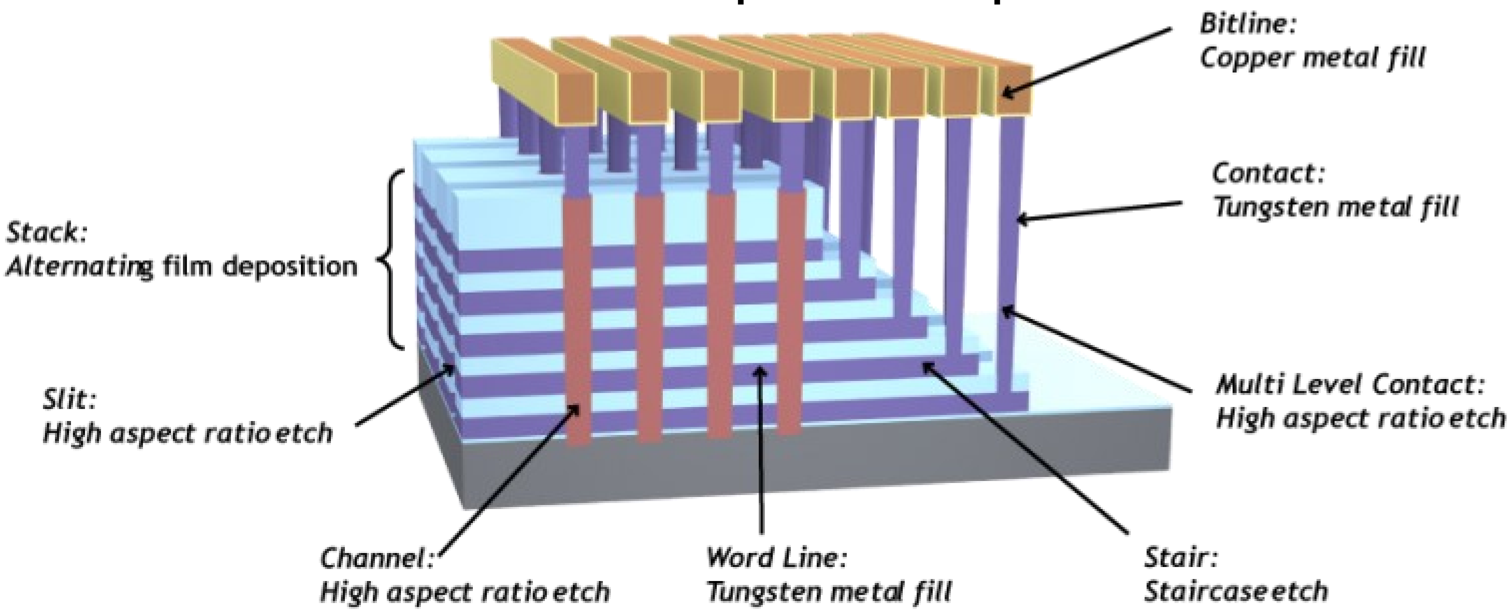
- Comparison of the computed amorphization profile for high energy ions (50 keV) of an As-implant process to the results obtained by Tian et al.

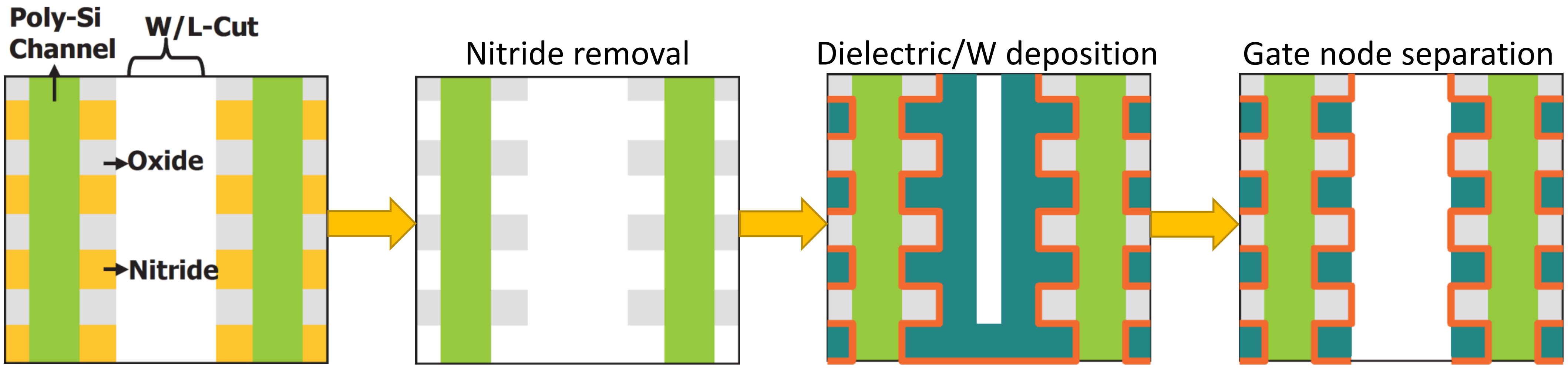
S. Tian et al., IEEE Transactions on Electron Devices 45(6), 1998

T. Reiter et al., IWCN 2022
T. Reiter et al., Solid-State Electronics 192, 2022

Process TCAD – SiO_2 Redeposition during 3D NAND Etching

- Fabrication of 3D NAND stacks can be quite complex

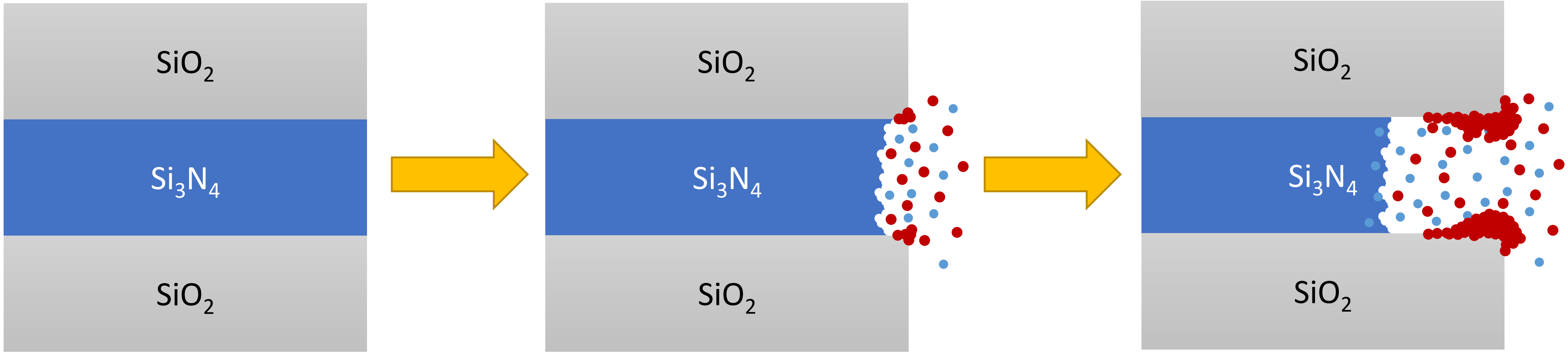




J. Jang et al., Proc. Symposium on VLSI Technology, 2009

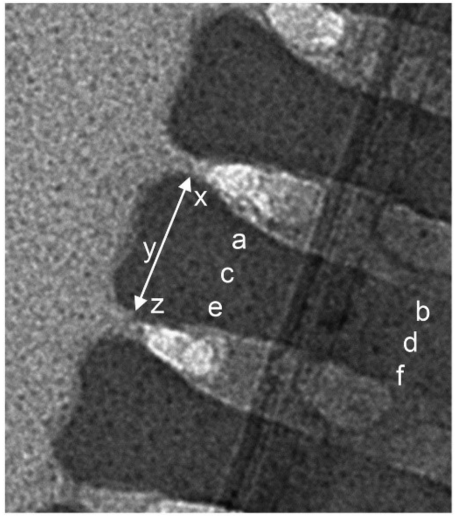
Process TCAD – SiO_2 Redeposition during 3D NAND Etching

- By-products deposit on the SiO_2 layers during Si_3N_4 etching in the 3D NAND stack



By-products (red circles) during Si_3N_4 (blue circles) etching

- Must consider
  - Etching of the Si_3N_4 layer (topography)
  - By-product generation at Si_3N_4/etchant interface during etching
  - Convective/diffusive transport of by-products (volume)
  - Deposition of by-products at etchant/SiO_2 interface (topography)



T. Reiter et al., Proc. SISPAD, 2023

T. Kim et al., Microelectronics Engineering, 2020

Process TCAD – SiO_2 Redeposition during 3D NAND Etching

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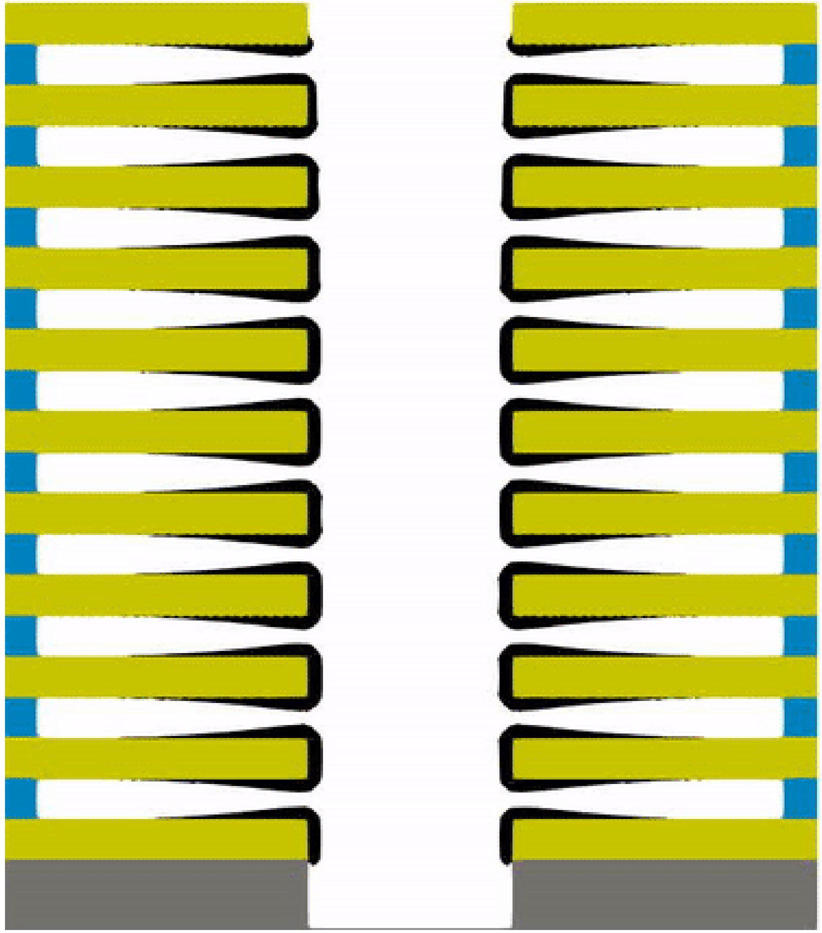
By-product accumulation

Convection-diffusion equation solution & accumulation of by-products



Final accumulated by-product

T. Reiter et al., Proc. SISPAD, 2023

Process TCAD – SiO_2 Redeposition during 3D NAND Etching

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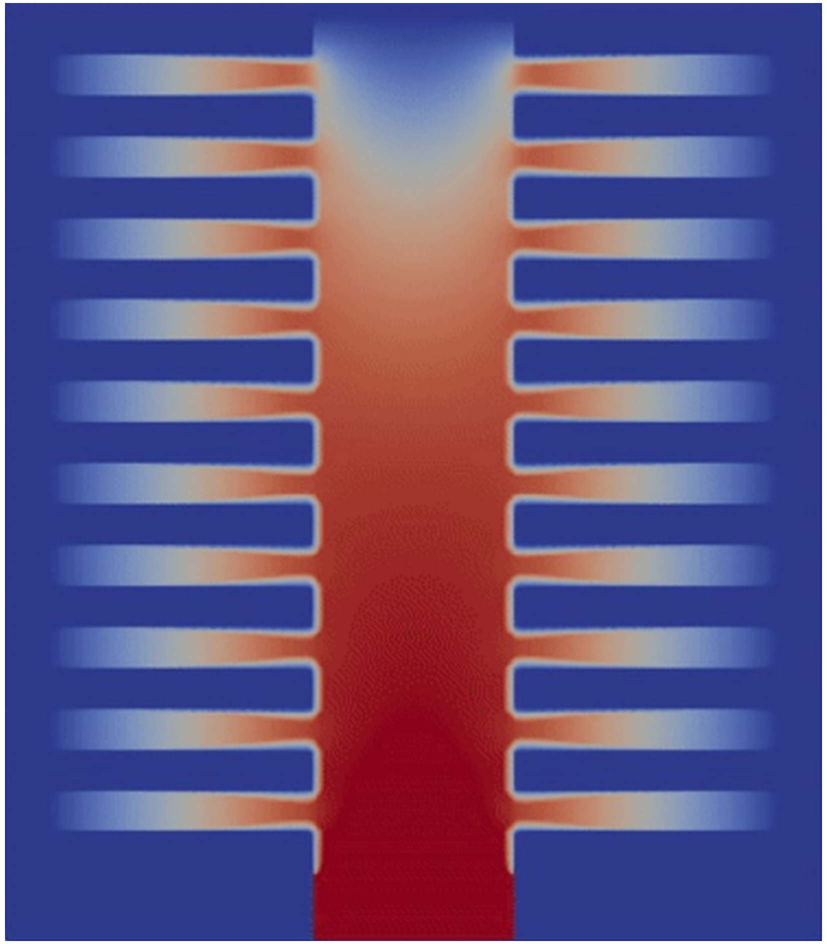
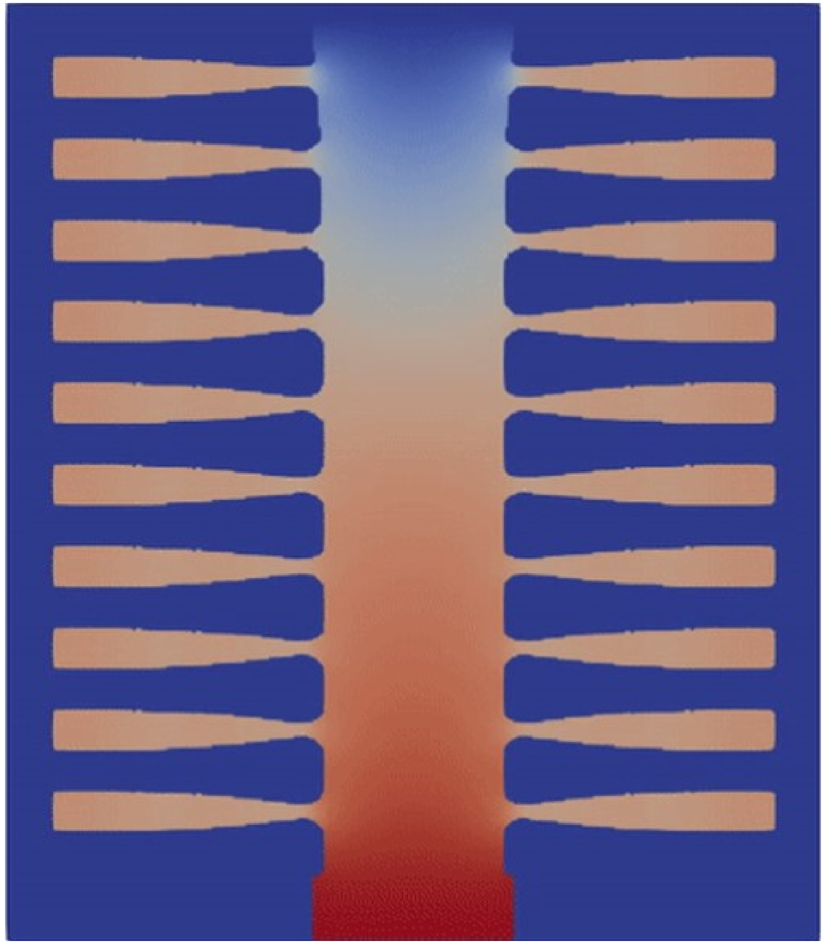
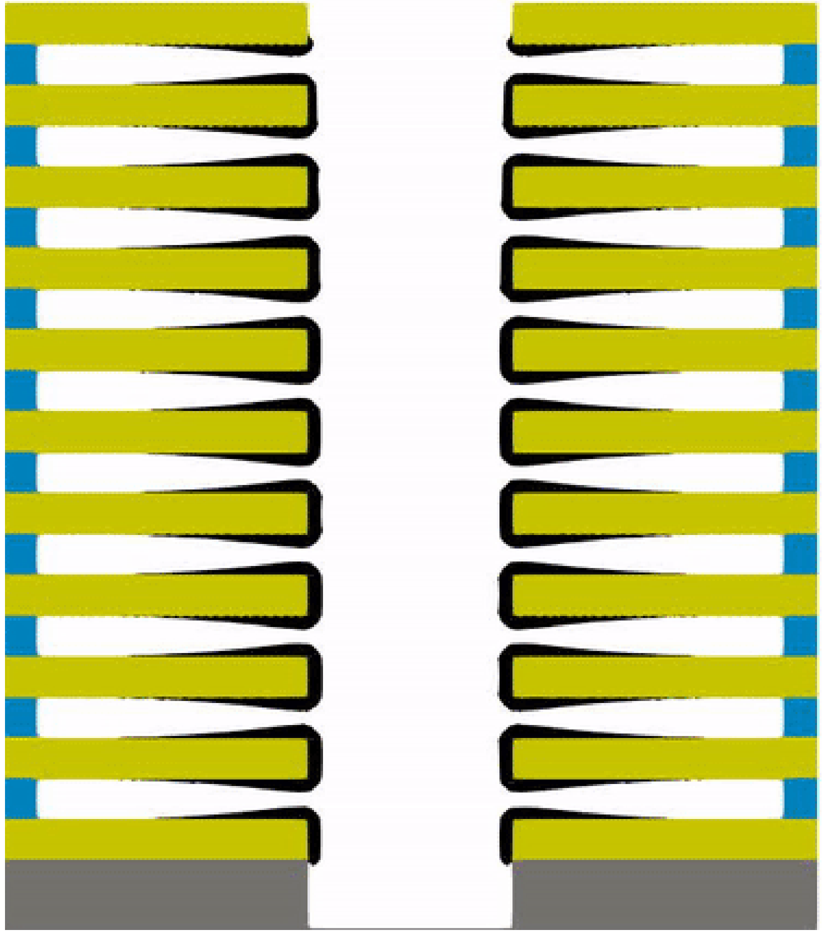


By-product accumulation



Convection-diffusion equation solution & accumulation of by-products

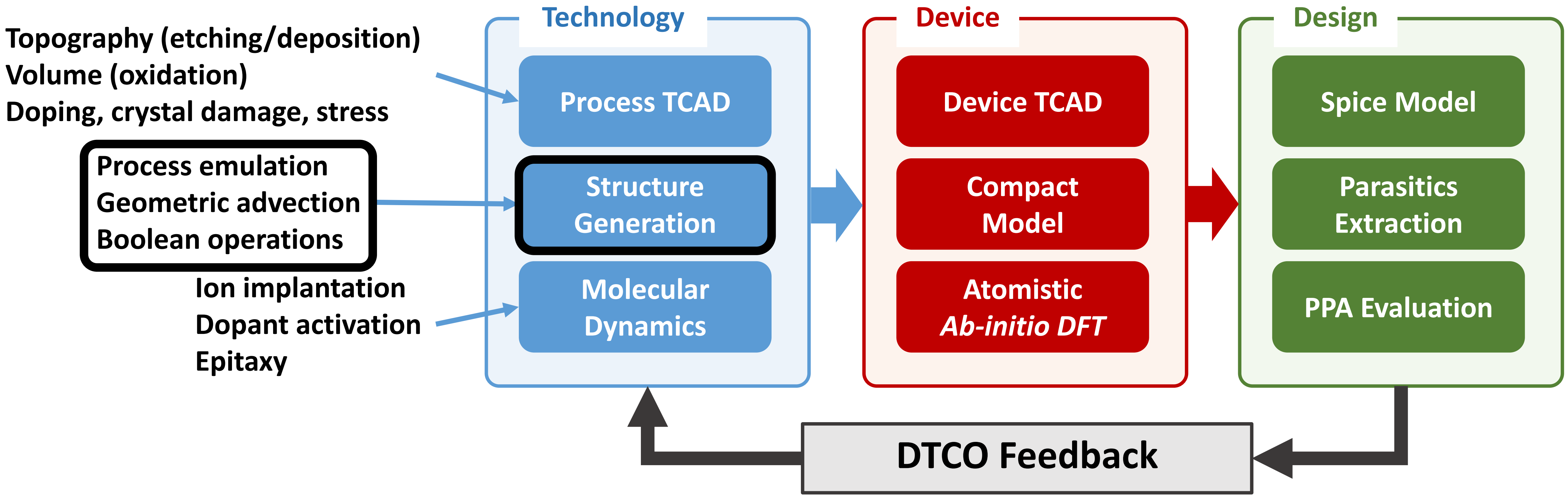


Final accumulated by-product

T. Reiter et al., Proc. SISPAD, 2023

Process TCAD – Emulation

- In the TCAD community, we like to think of it as a flow with a feedback loop



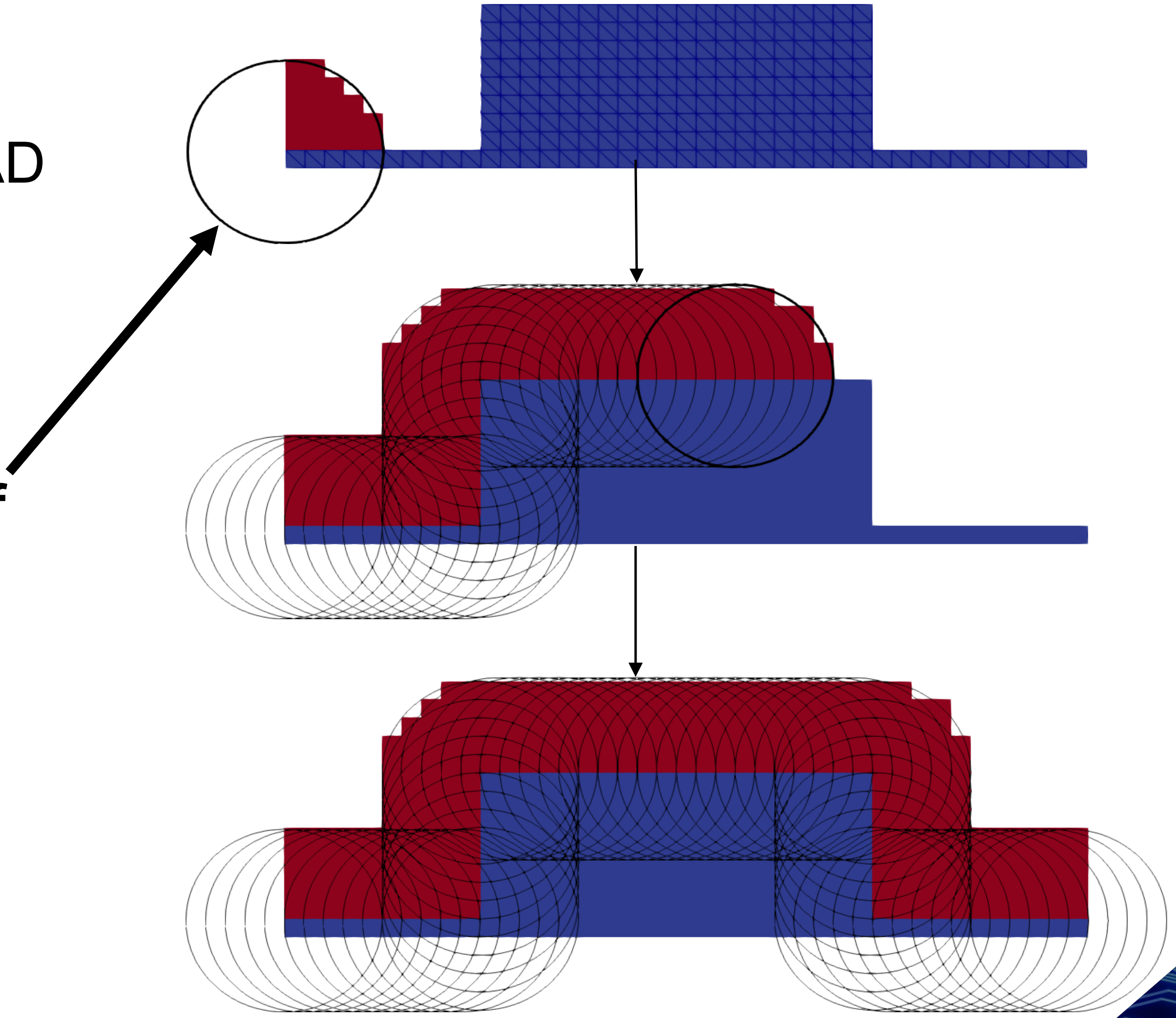
Process Emulation – Generating a Process-Aware Structure

Process emulation:

- Fast geometric representation
- Can provide a direct link to device TCAD
- Models are empirical and not physical
- Missing link to fabrication parameters

Set of rules to determine the shape of this distribution function based on

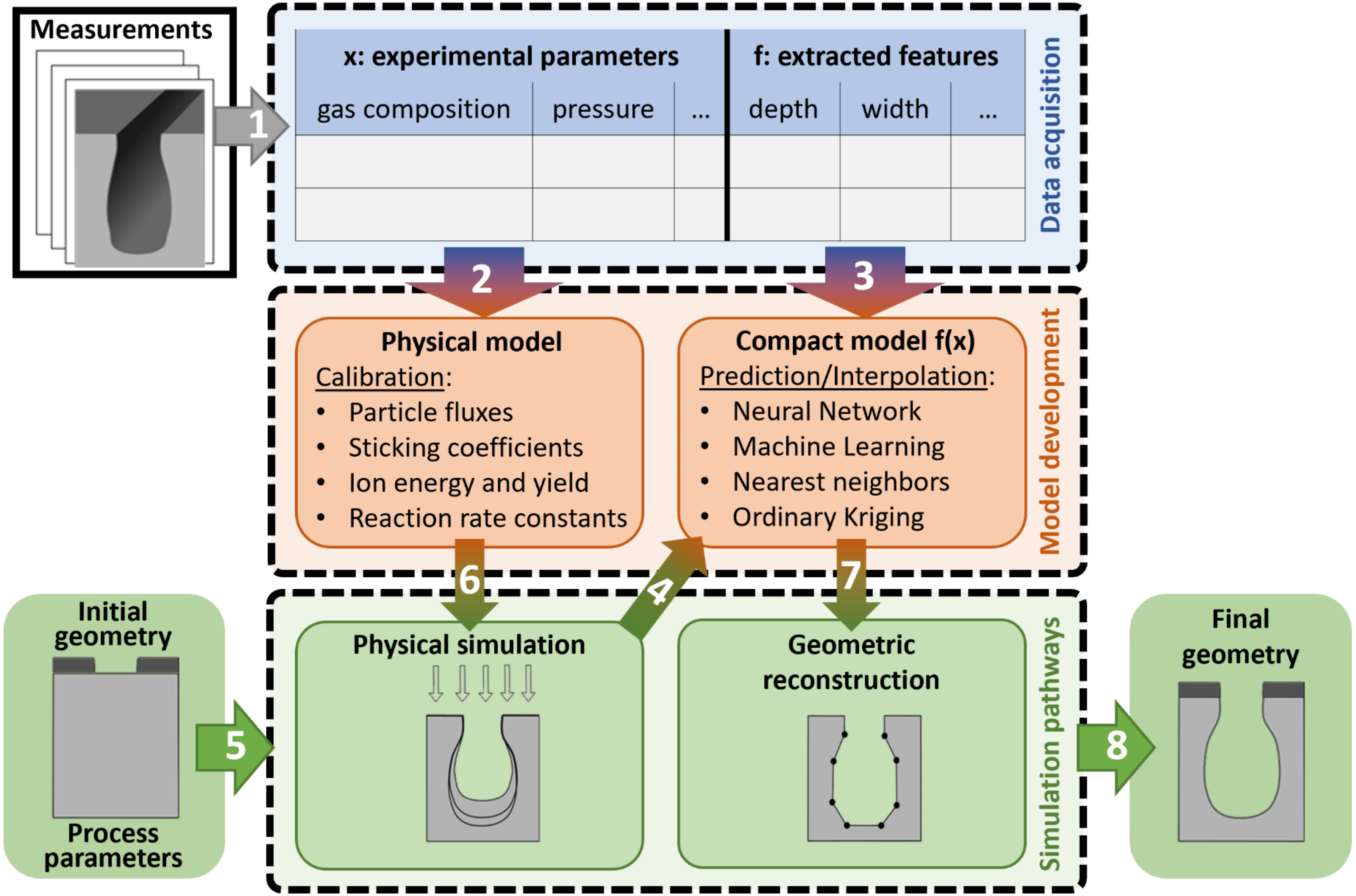
- Process parameters
  (time, directionality, thickness, etc.)
- Geometry
  (curvature, corners, edges, etc.)



X. Klemenschits et al., Computer Methods in Applied Mechanics and Engineering, 2021

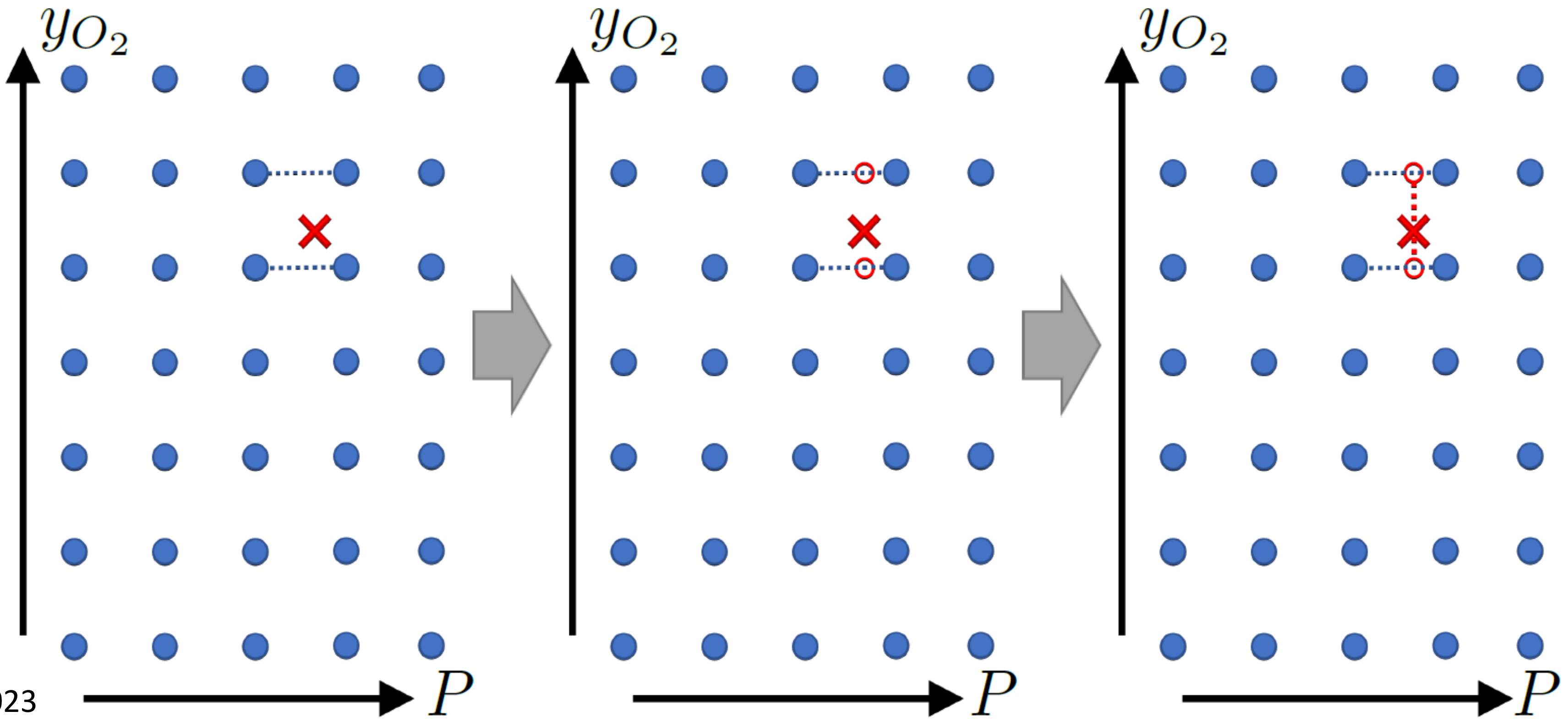
Process Emulation – Generating a Process-Aware Structure

- We use a combination of measurements and physical simulations to design geometric/compact models



Process Emulation – Compact Model for Etching in SF_6/O_2 Plasma

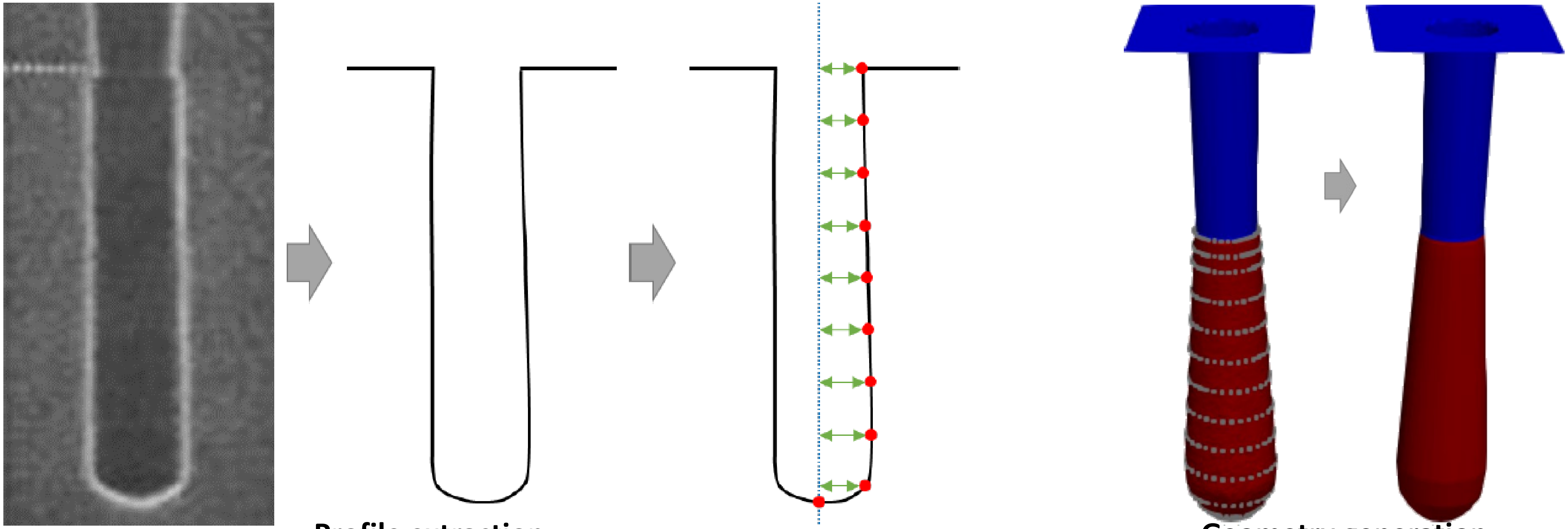
- We use a combination of measurements (bold) and physics-based simulations to design geometric/compact models
- Example: SF_6/O_2 plasma etching using 35 data points
  - Oxygen gas fraction in feed, with respect to SF_6, y_{O_2} (**0.44**, **0.5**, 0.53, **0.56**, 0.58, 0.6, **0.63**)
  - Pressure in the plasma chamber, P (**10**, 17.5, **25**, 32.5, **40**)
  - Tested 80 random locations in the 2D space to assess accuracy and speed



L. Filipovic et al., SISPAD 2023

Process Emulation – Compact Model for Etching in SF_6/O_2 Plasma

- Profile extraction and subsequent generation during compact modeling



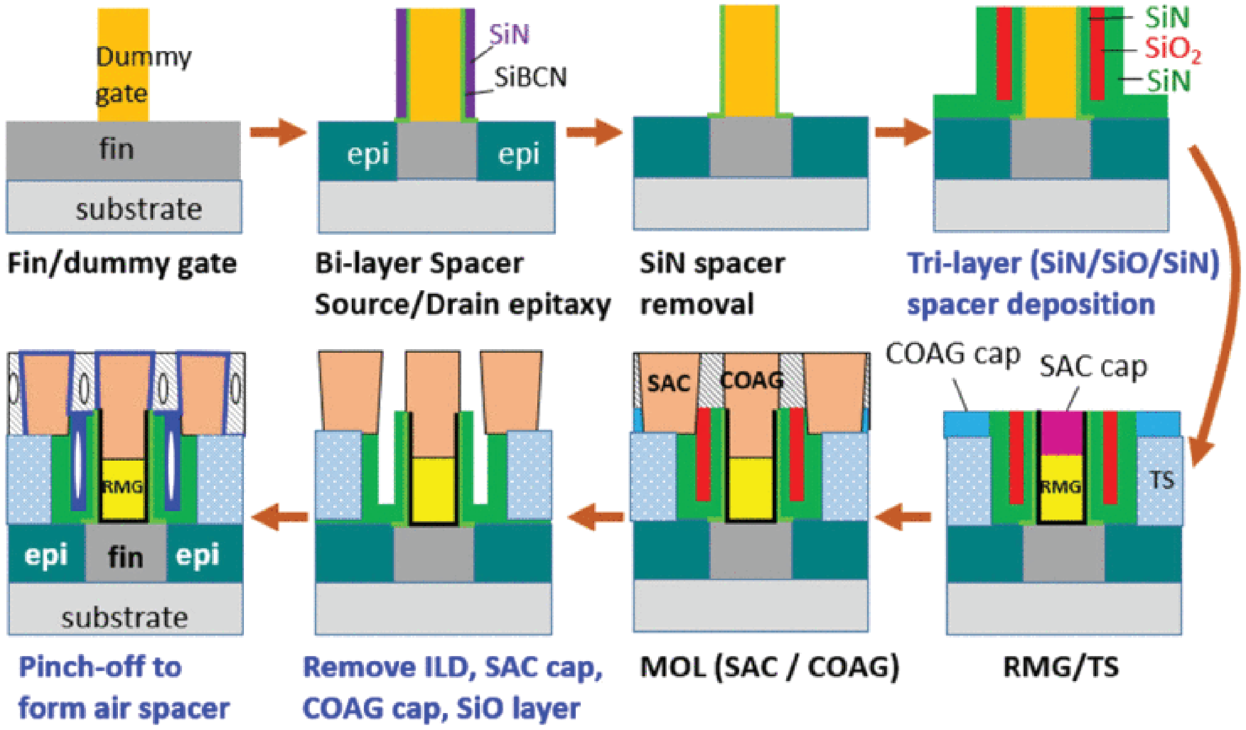
Profile extraction **Geometry generation**

- Compact model is ~2k times faster on single core (compared to physical model on 40 cores)
- Average (maximum) error in depth and width-at-half-depth is 2% and 1% (6.2%)

Process Emulation – Compact Model for DTCO

- Study of the impact of air spacers at N7

- Fin formation
- Dummy gate
- Sacrificial S/D epi spacer
- S/D epitaxy
- S/D epi spacer removal
- Sacrificial ILD
- Replacement HK/MG
- SAC/COAG contacts
- Air spacer module
  - Remove sacrificial ILD
  - Remove gate and trench silicide caps
  - Deposit non-conformal dielectric to pinch-off and form the AS
  - Deposit new ILD
  - Planarization
- BEOL

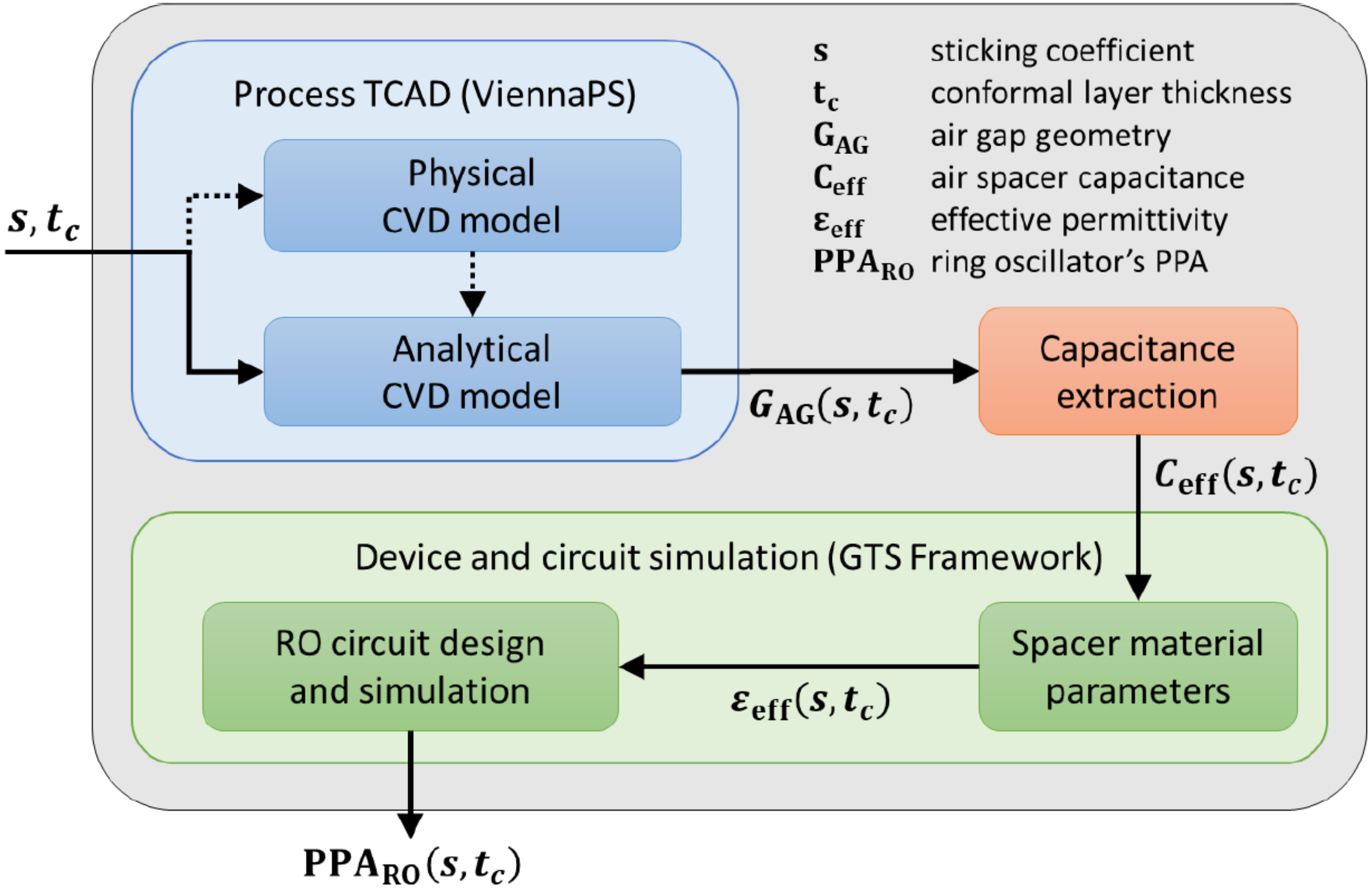


- Air spacer (AS) is formed after MOL
- Conforms to self-aligned contact (SAC) and contact over active gate (COAG)

K.Cheng et al., IEEE TED 2020

Process Emulation – Compact Model for DTCO

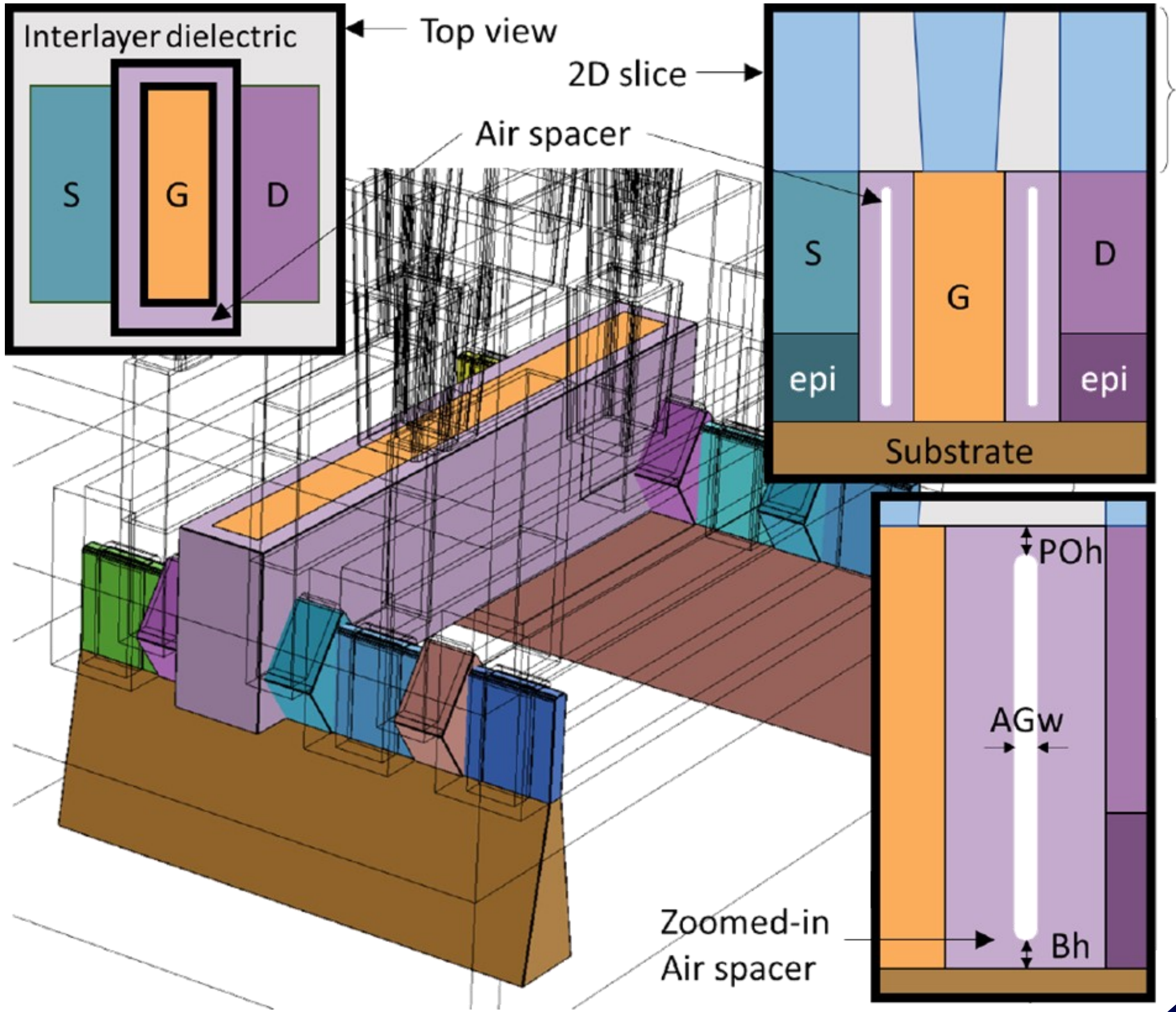
- Study of the impact of air spacers at N7
- Apply air spacers to transistors in a 5-stage ring oscillator circuit
- Implement a full DTCO flow



Process Emulation – Compact Model for DTCO

- Study of the impact of air spacers at N7
- Apply air spacers to transistors in a 5-stage ring oscillator circuit

- For a "compact model" we need a geometrical description of the air gap inside the spacer
  - POh – pinch-off height
  - Bh – bottom height
  - AGw – air-gap width

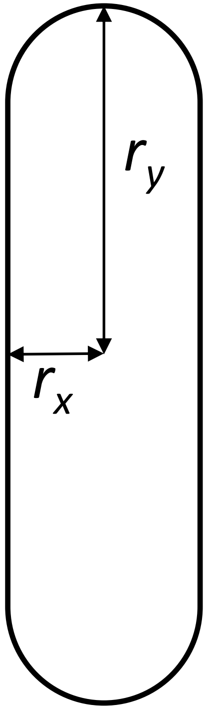


L. Filipovic et al., SISPAD 2022

Process Emulation – Compact Model for DTCO

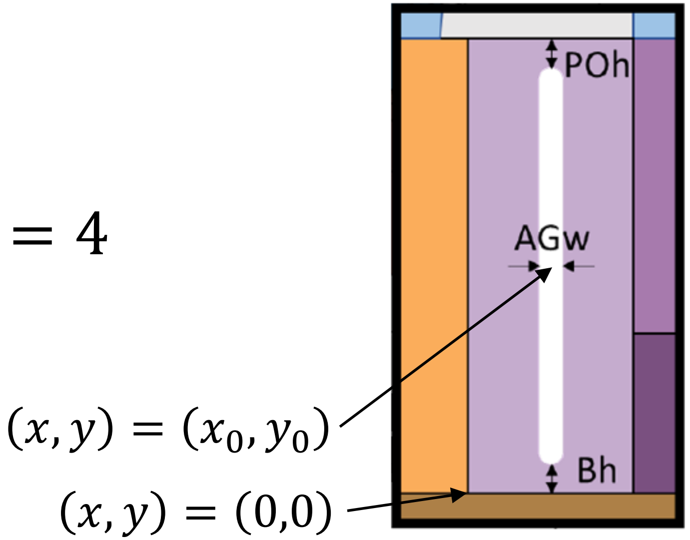
- Study of the impact of air spacers at N7
- Apply air spacers to transistors in a 5-stage ring oscillator circuit

$$\frac{(y-y_0)^4}{r_y^4}+\frac{(x-x_0)^4}{r_x^4}=1$$



- For a "compact model" we need a geometrical description of the air gap inside the spacer
  - POh – pinch-off height
  - Bh – bottom height
  - AGw – air-gap width
- Linear interpolation for sticking coefficient *s* and conformal SiN thickness t_c
- Air gap shape is represented using a superellipse with $n = 4$

$$r_x=\frac{AGw}{2} \qquad r_y=\frac{h_s-POh-Bh}{2} \qquad x_0=r_x+t_c \qquad y_0=r_y+Bh$$



L. Filipovic et al., SISPAD 2022

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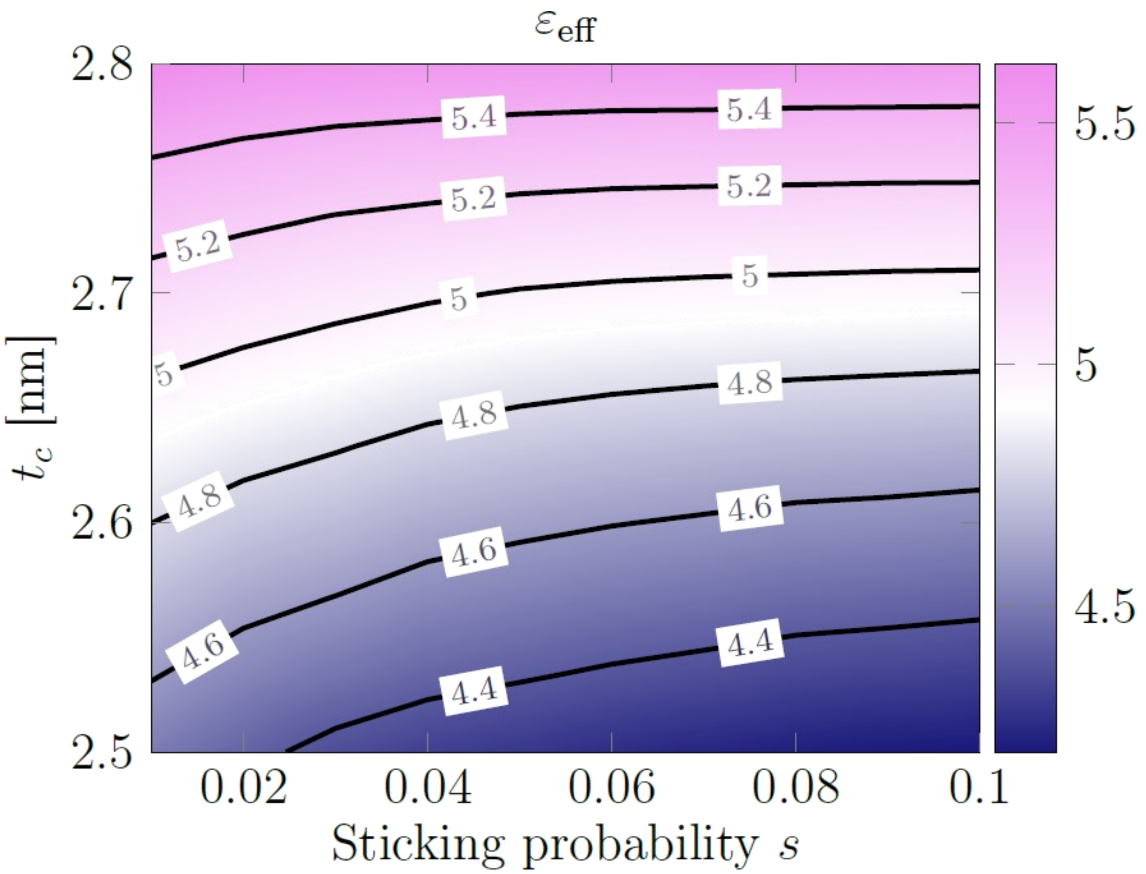
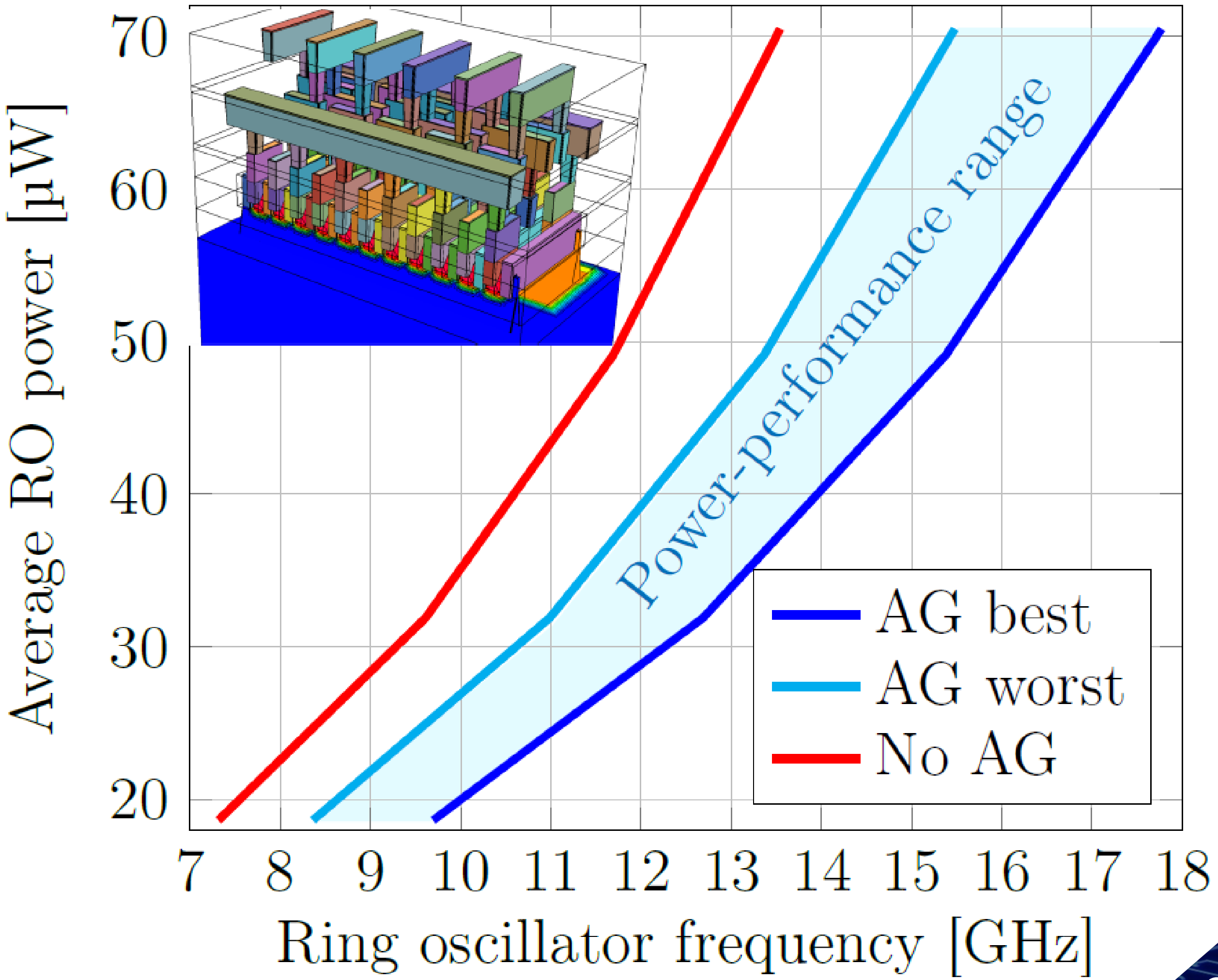
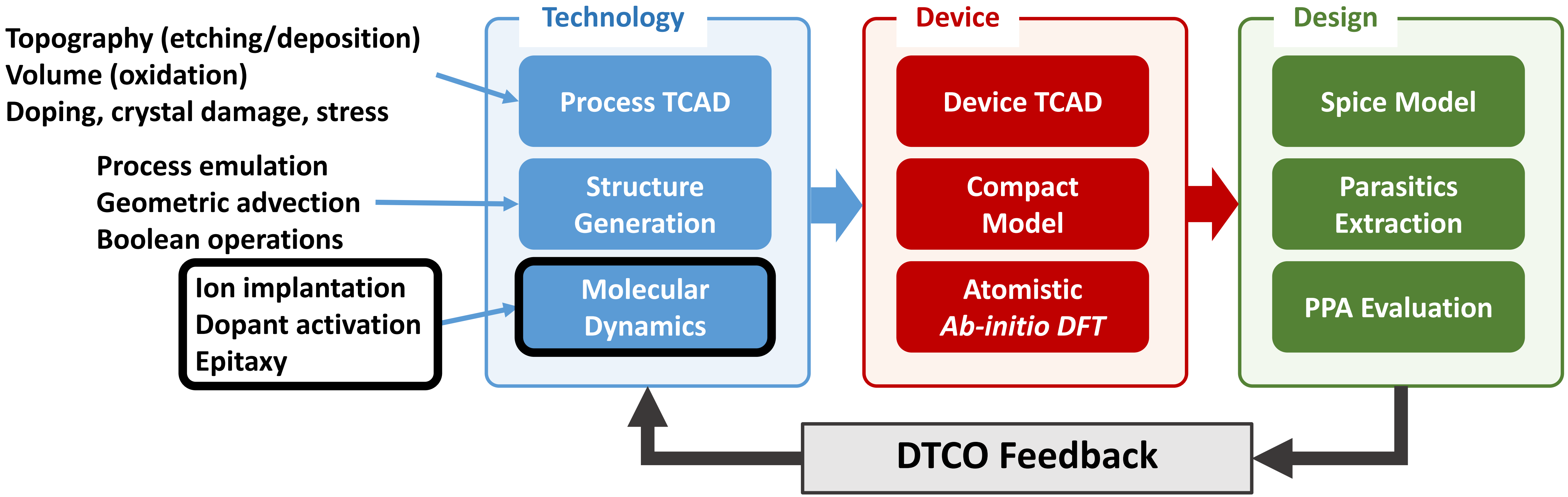




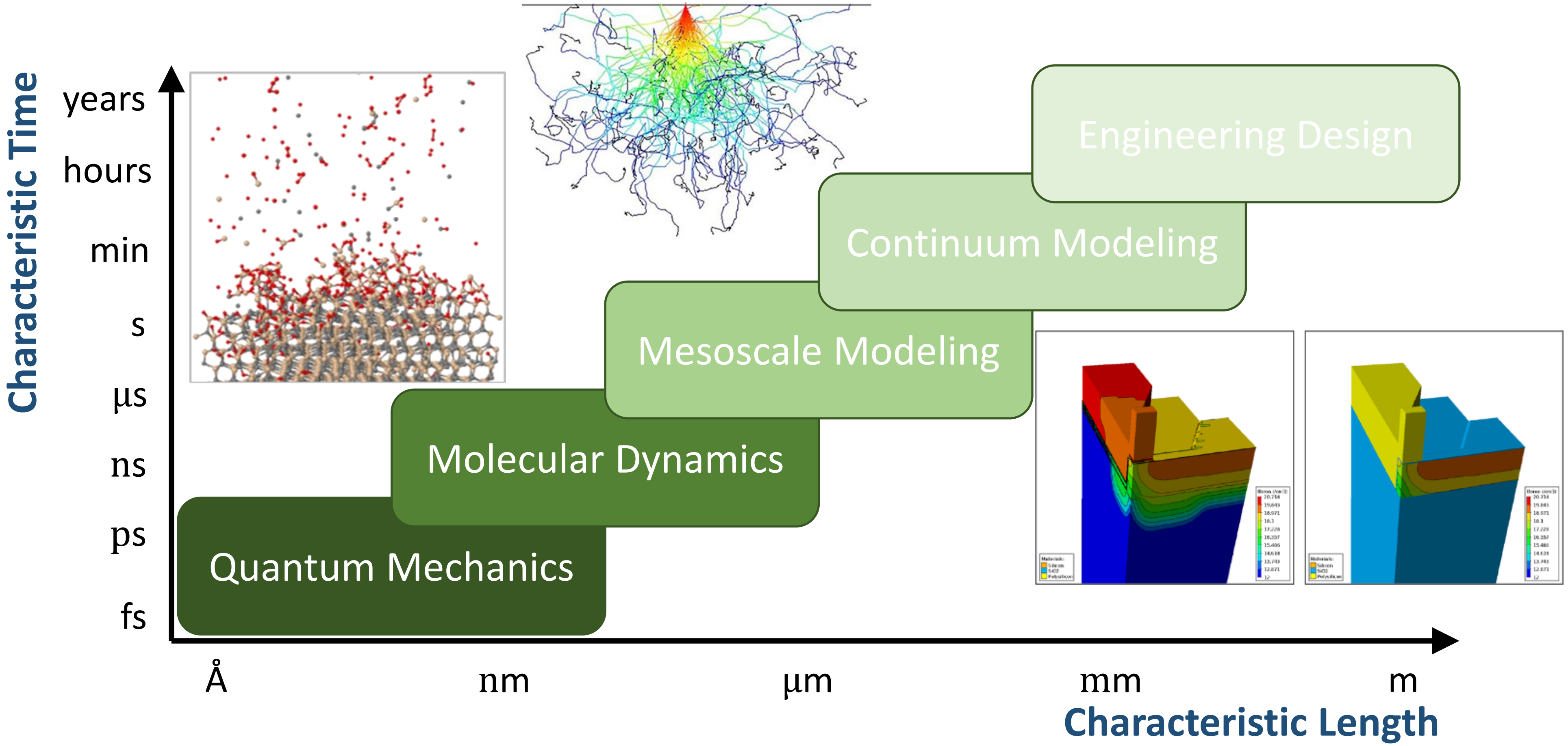
Process TCAD – Multi-Scale Modeling

- In the TCAD community, we like to think of it as a flow with a feedback loop

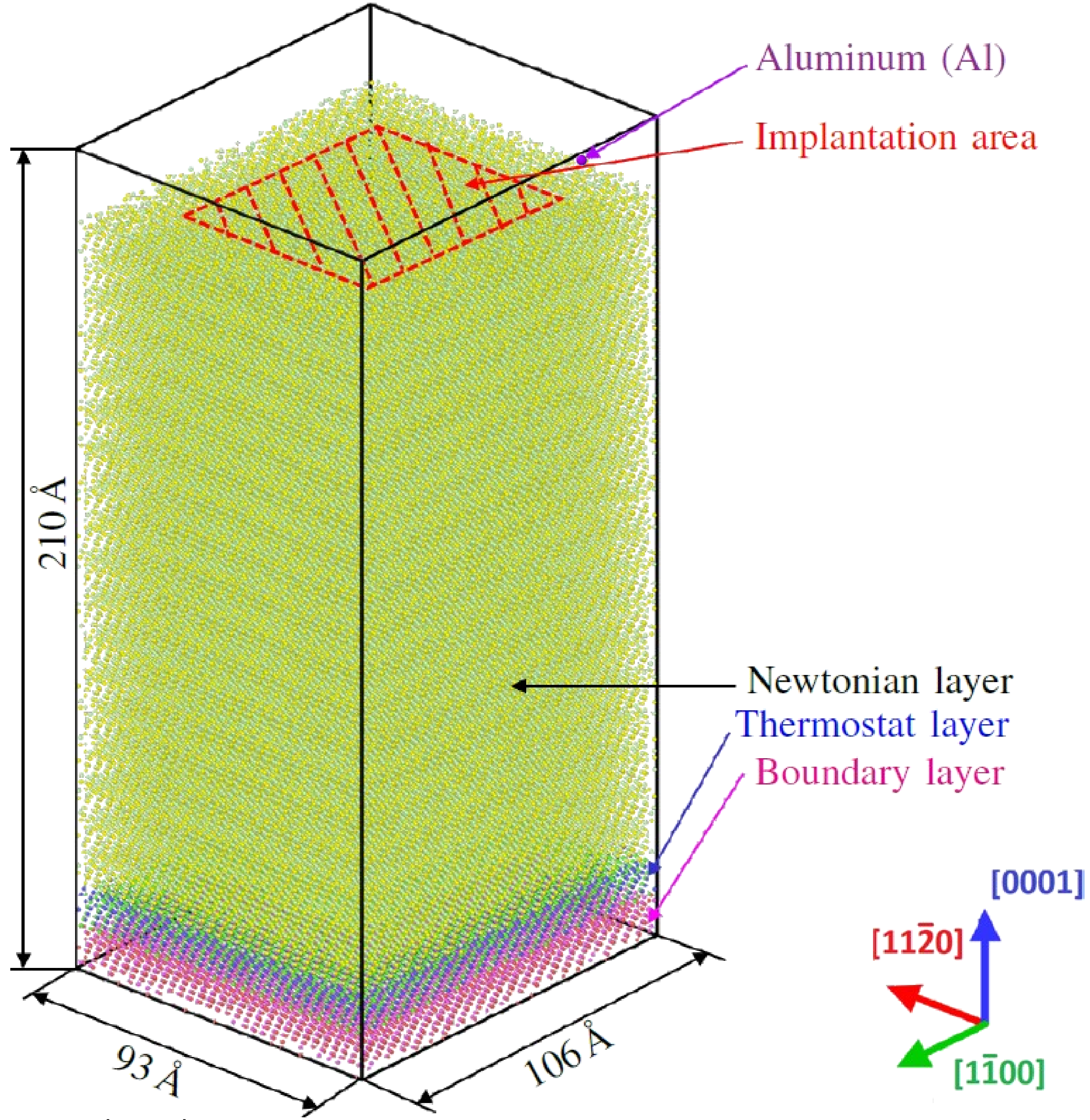


Multi-Scale Modeling – Molecular Dynamics

- Introducing new materials within DTCO is no easy task
- There is a lack of experimental data, especially compared to silicon
- Atomistic level simulations are imperative



Molecular Dynamics Modeling – Al-Implantation in SiC

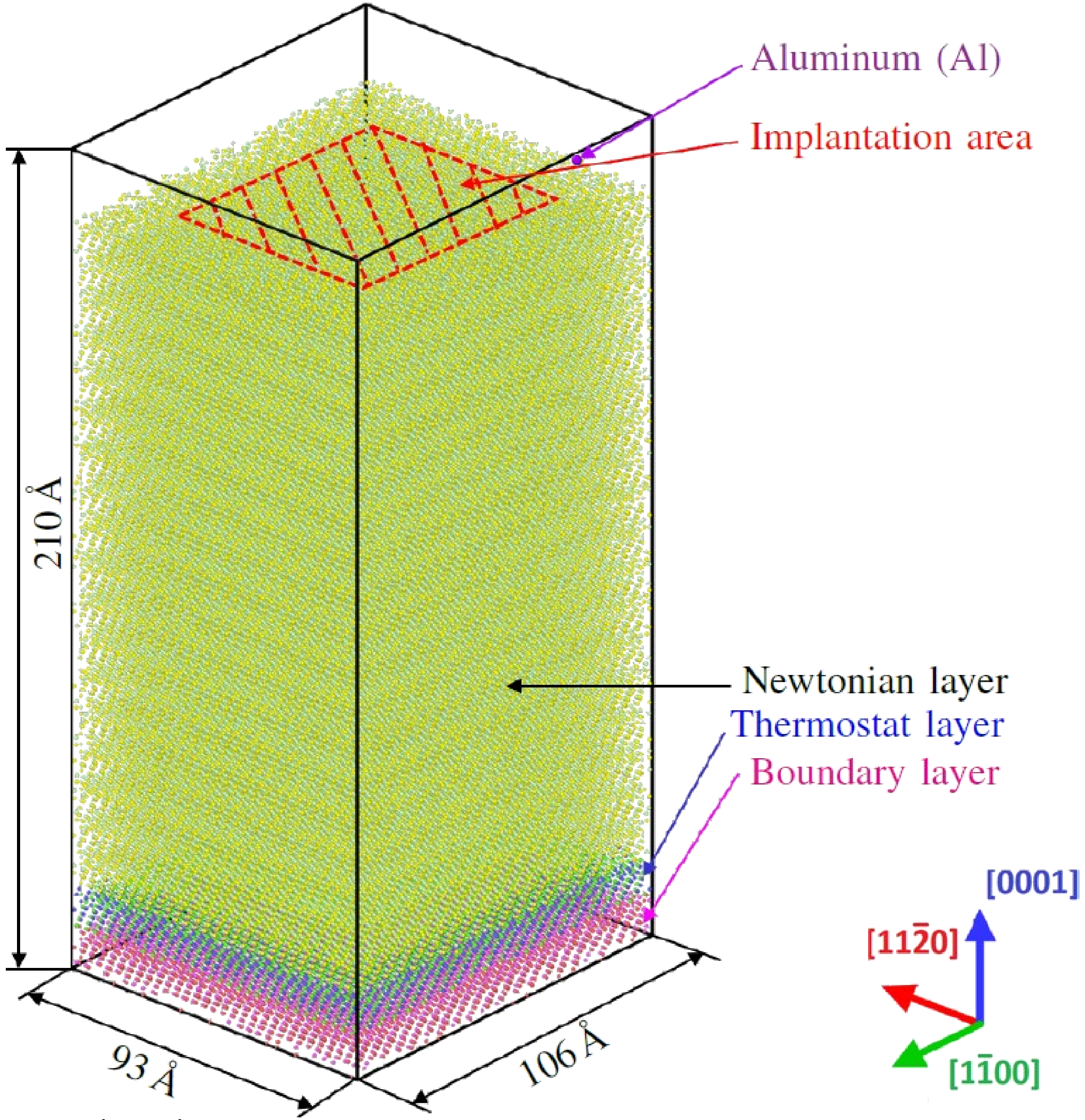


S. Leroch et al., SISPAD 2023

- Work piece: 9.3nm × 10.6nm × 21nm
- Incident angle of Al: 7°
- Implant energy: 2 keV
- Doses: 5×10^{13}cm^{-2} & 5×10^{14}cm^{-2}
- Implant temperatures: 300K & 800K
- Which interatomic potential to use?
  - Formation & migration energies:

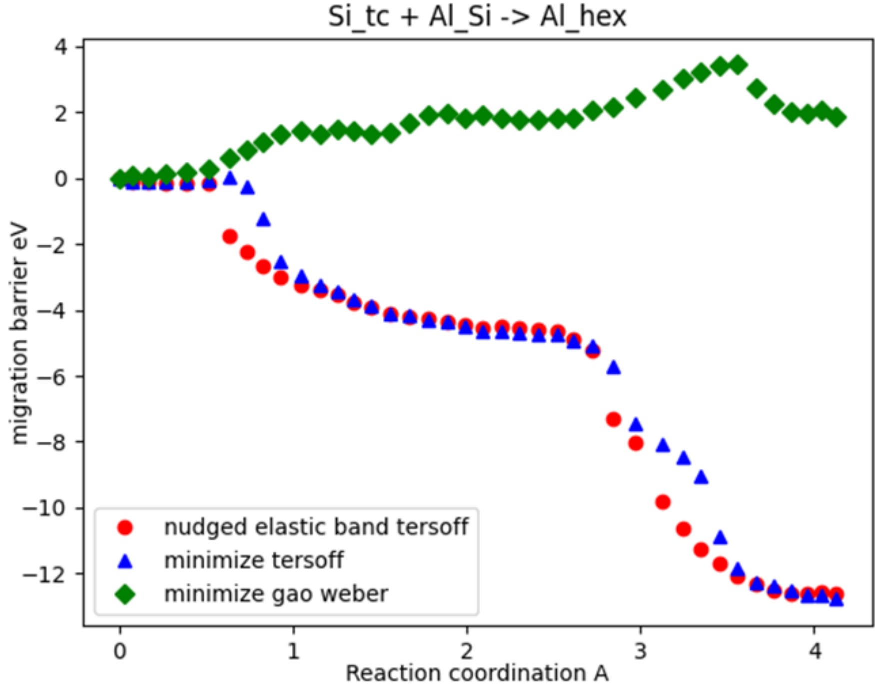
Defect	Gao-Weber (eV)	Tersoff (eV)	DFT (eV)
Al_{TSi_k}	5.39	7.9	8.26
Al_{TC_k}	5.638	5.93	6.12
Al_{Si}	1.58	5.02	1.36
Al_{Si}+V_C	3.54	7.76	3.28
Al_{hex}	3.68	4.87	8.5
Al_{Si}+Si_{hex}	4.61	17.28	9.2
Al_{Si}+Si_{TC}	2.96	17.82	7.29

Molecular Dynamics Modeling – Al-Implantation in SiC



Migration barrier

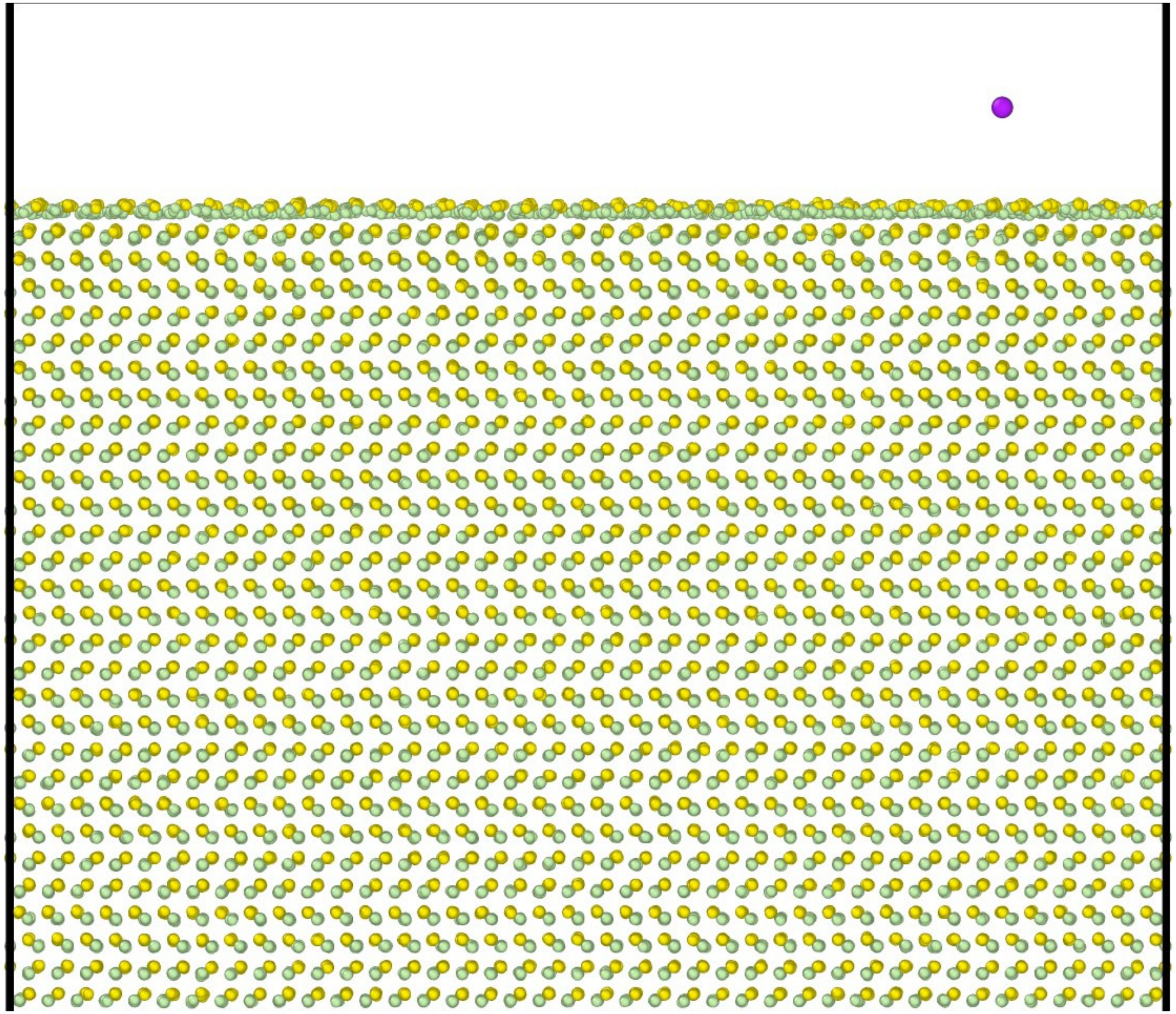
- Kick-out process of Al from Al_{Si} to the hexagonal interstitial Al_{hex} with the assistance of a Si interstitial Si_{TC}
- **DFT – Kick-out 3.8 eV**
- Tersoff – Kick-in 12.5 eV
- Gao-Weber – Kick-out 3.1 eV



S. Leroch et al., SISPAD 2023

Molecular Dynamics Modeling – Al-Implantation in SiC

- Simulation of Al implantation in SiC – 10ps between Al atom impingement



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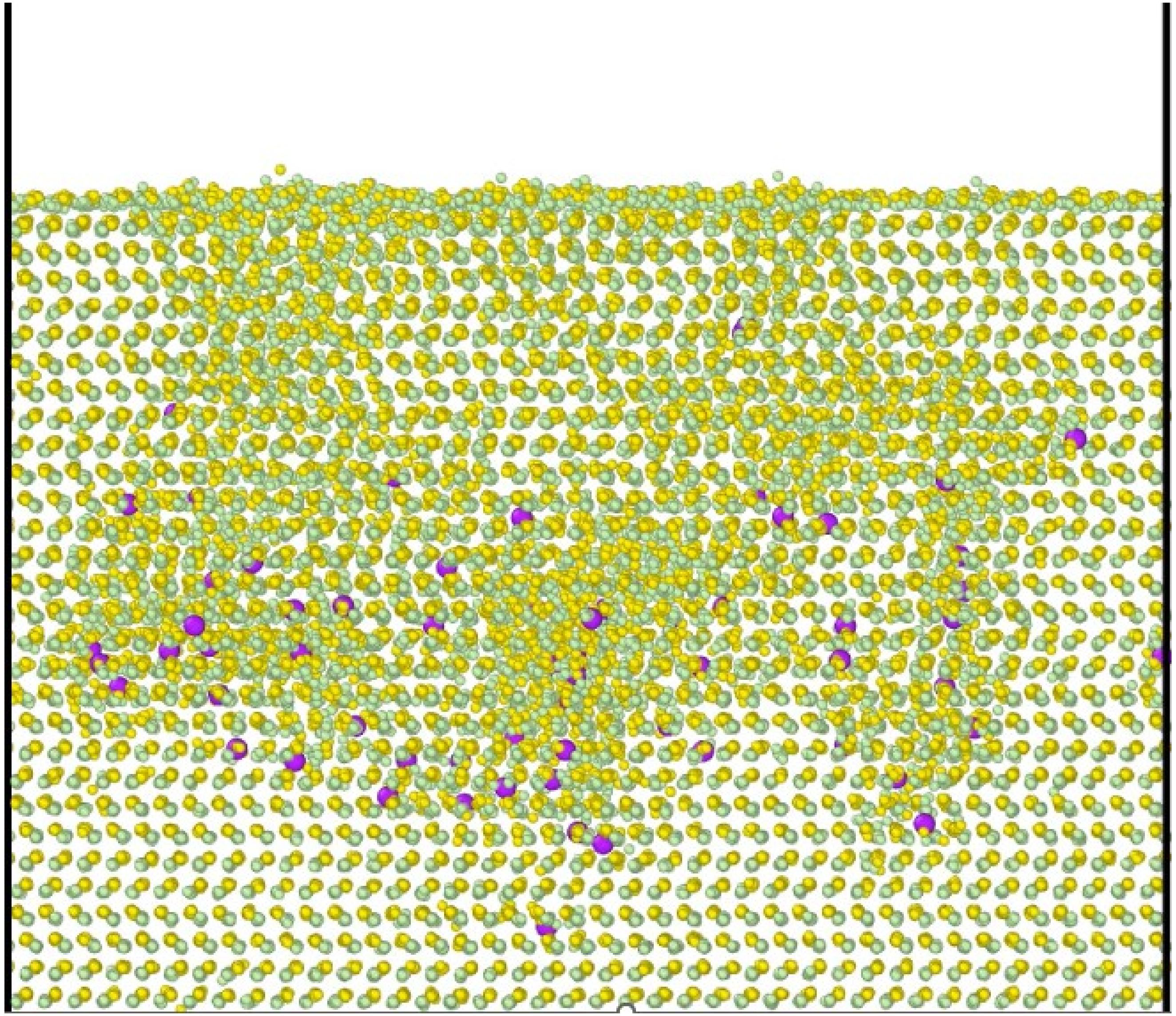

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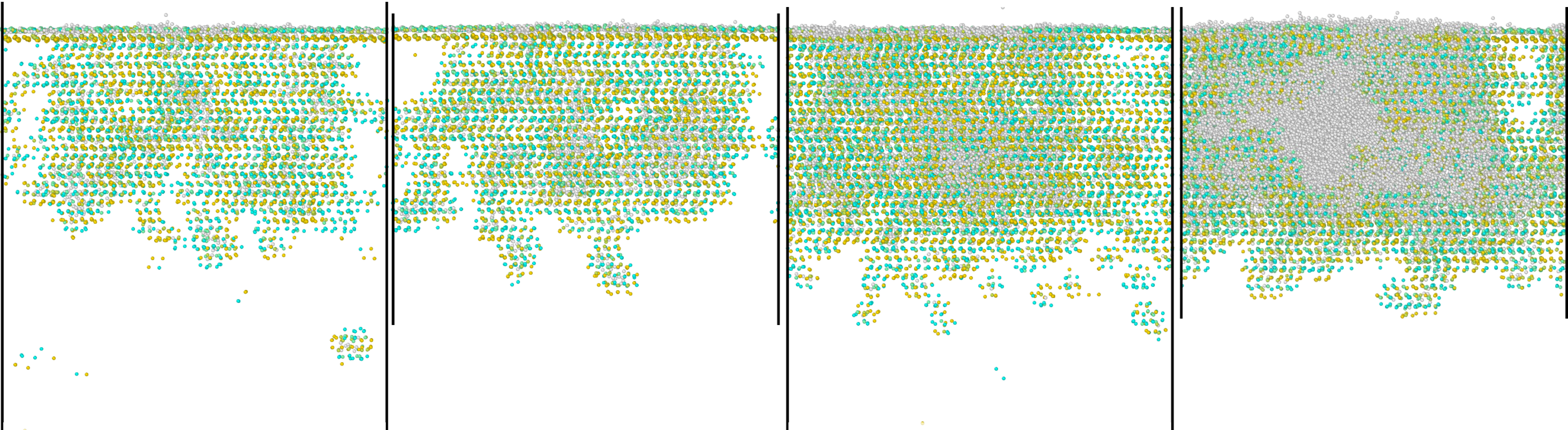
Molecular Dynamics Modeling – Al-Implantation in SiC

- Simulation of Al implantation in SiC – Resulting amorphous clusters



800K, 5×10^{13}cm^{-2} | 300K, 5×10^{13}cm^{-2} | 800K, 5×10^{14}cm^{-2} | 300K, 5×10^{14}cm^{-2}

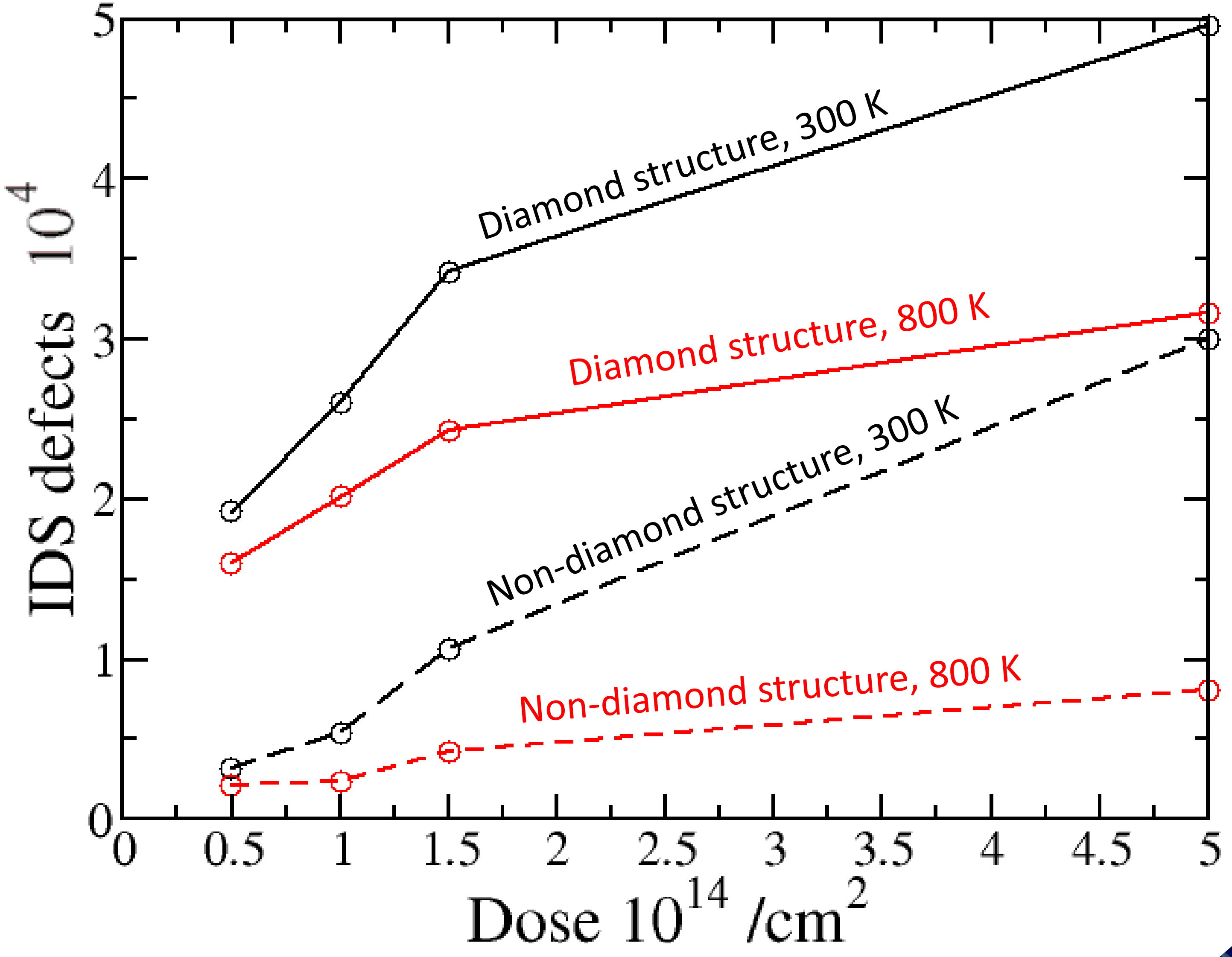
- Temperature has a higher impact at larger implant doses

S. Leroch et al., SISPAD 2023

Molecular Dynamics Modeling – Al-Implantation in SiC

- Simulation of Al implantation in SiC – Resulting amorphous clusters

- Defects can be interstitials, antisites, and vacancies



S. Leroch et al., SISPAD 2023

Conclusion

- Process simulations have an increasing role in the design of novel micro- and nano-electronic devices and circuits through DTCO
- Process simulation encompasses many types of simulations:
  - Geometry: Topography and/or volume
  - Accuracy: Physics-based models and/or geometric emulation/compact models
  - Time and size scales: From molecular dynamics to continuum
- At the end of the day, trade-offs must be made
- Importance for *useful* models lies in…
  - Predictivity, process-aware geometries for DTCO, introduction of new materials

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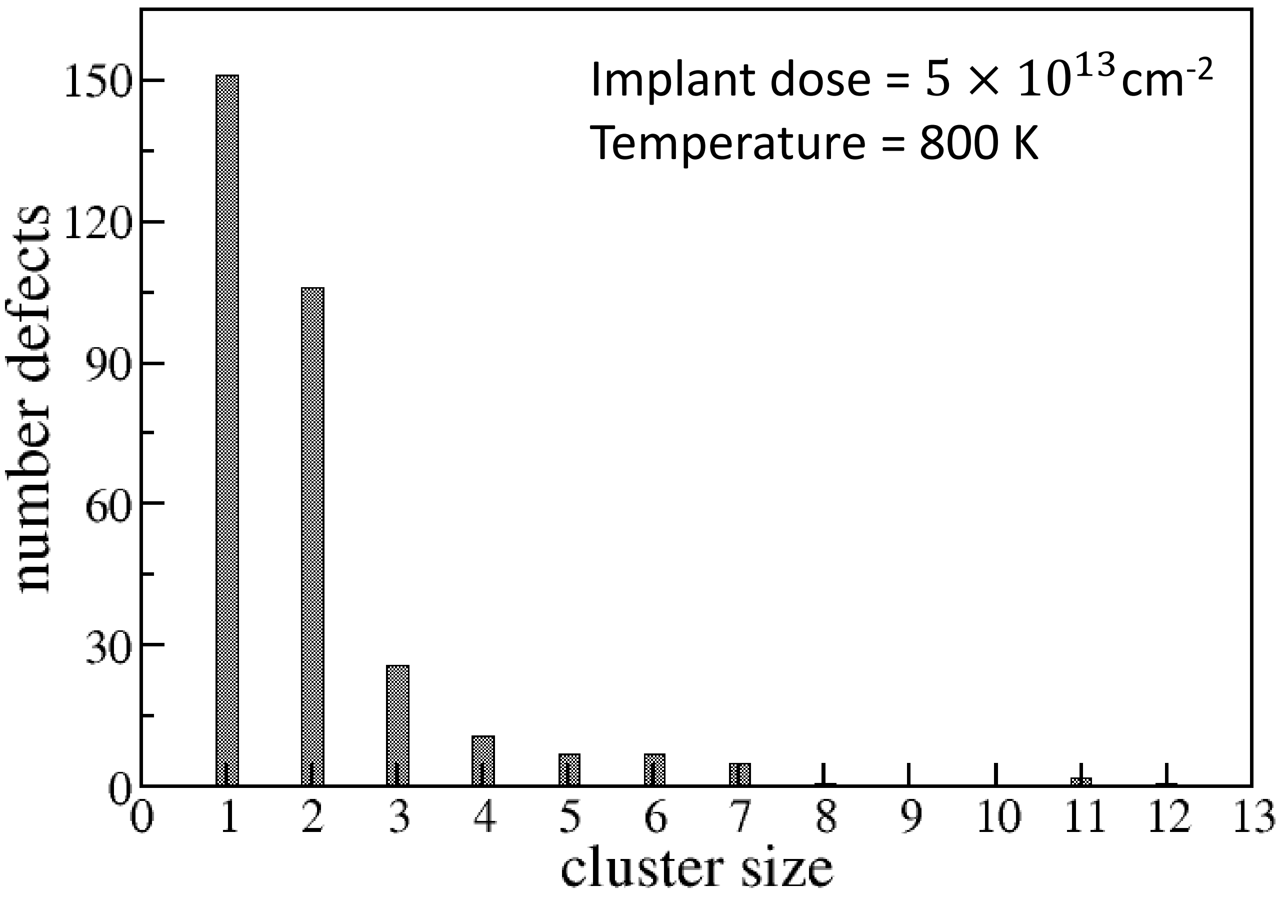
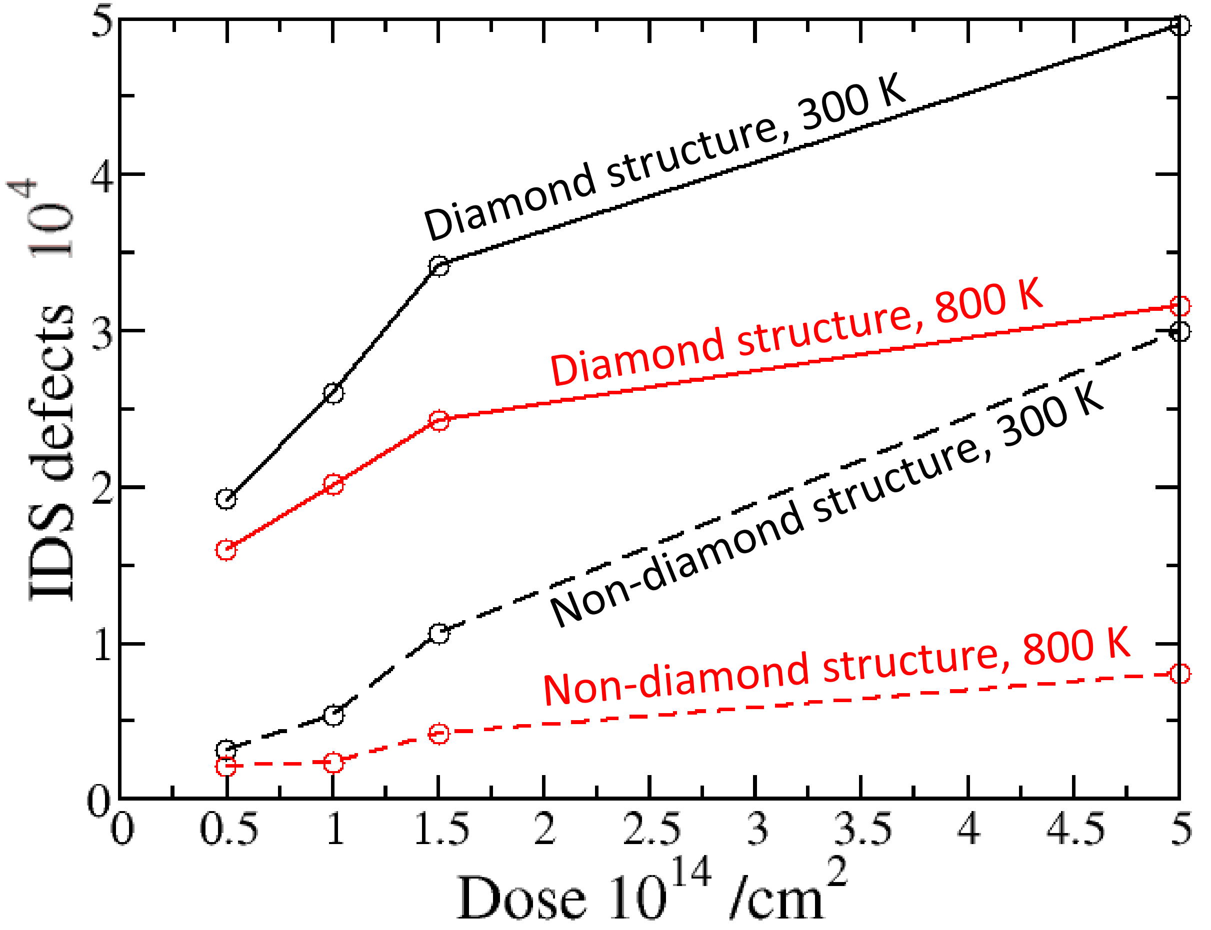
Molecular Dynamics Modeling – Al-Implantation in SiC

- Simulation of Al implantation in SiC – Resulting amorphous clusters





- Defects can be interstitials, antisites, and vacancies

S. Leroch et al., SISPAD 2023