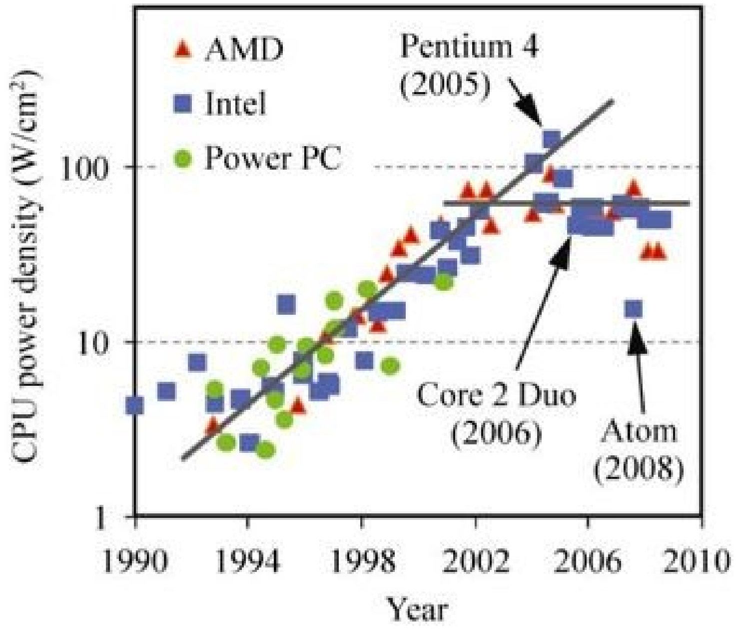
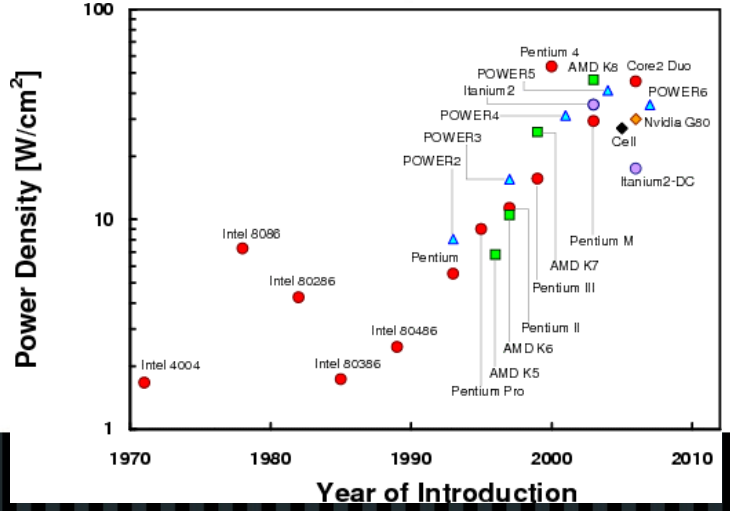
Electro-thermal Properties of 2D Materials

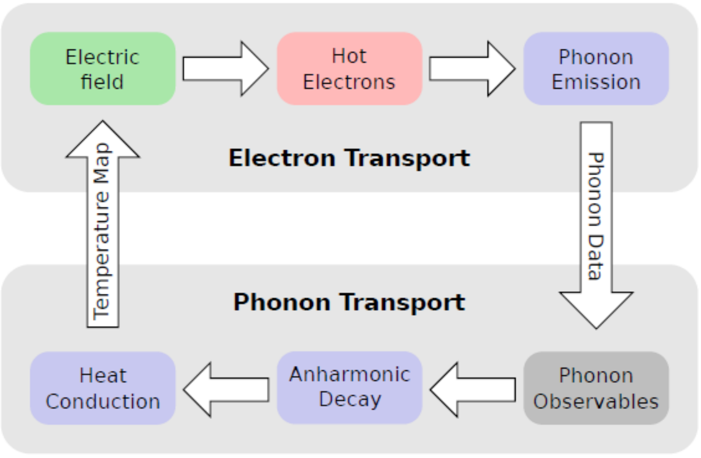
Zlatan Aksamija
Associate Professor, Materials Science and Engineering
NanoEnergy Lab, University of Utah
zlatan.aksamija@utah.edu
https://nanoenergy.mse.utah.edu

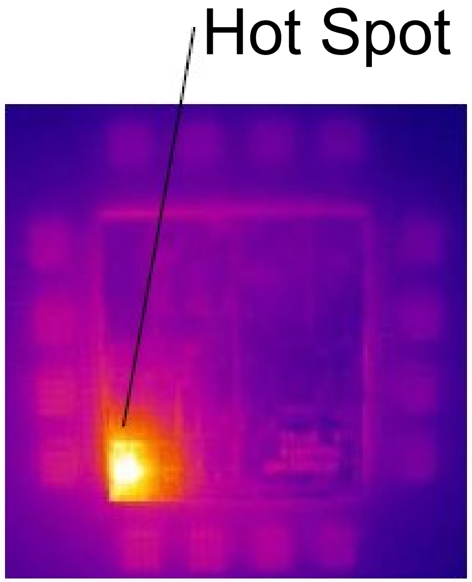
NanoEnergy Lab, MSE@Utah

Heat dissipation: a bottleneck to scaling









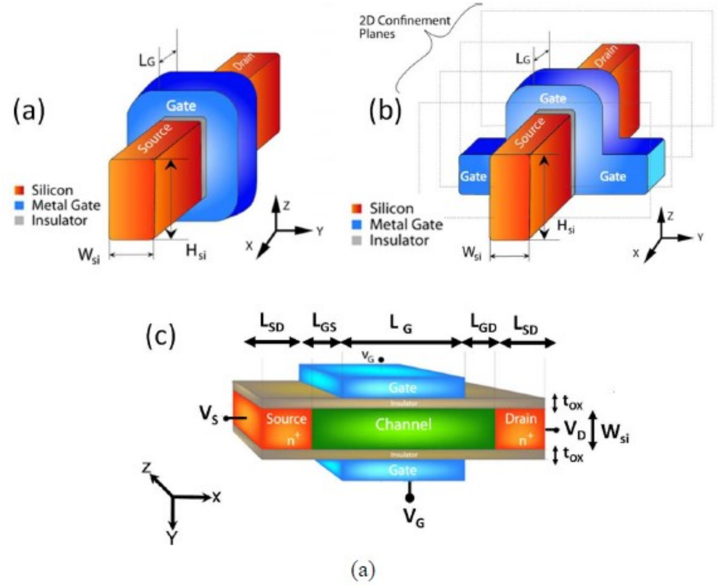
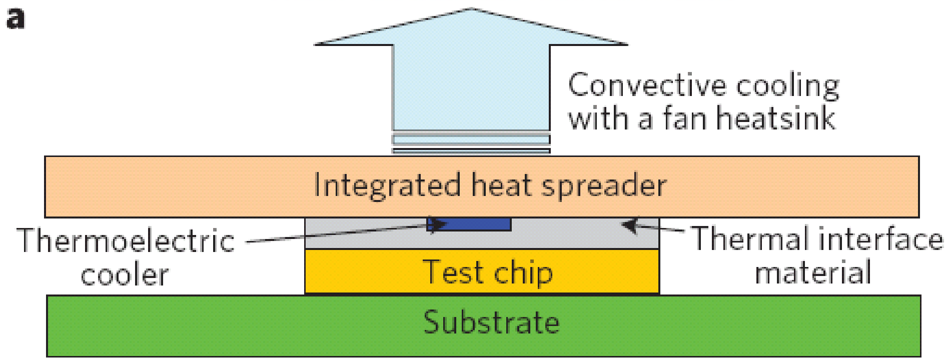
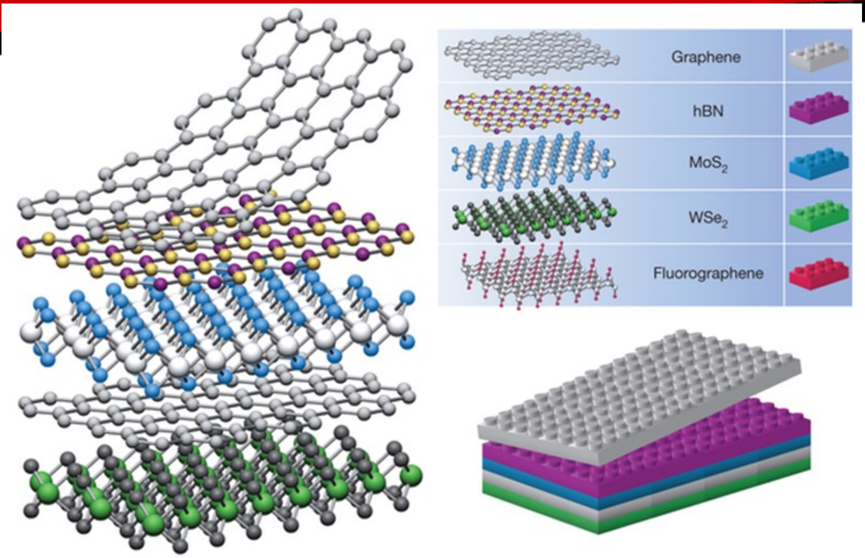


Fig. 4: Schematic of DG,TG and GAA.

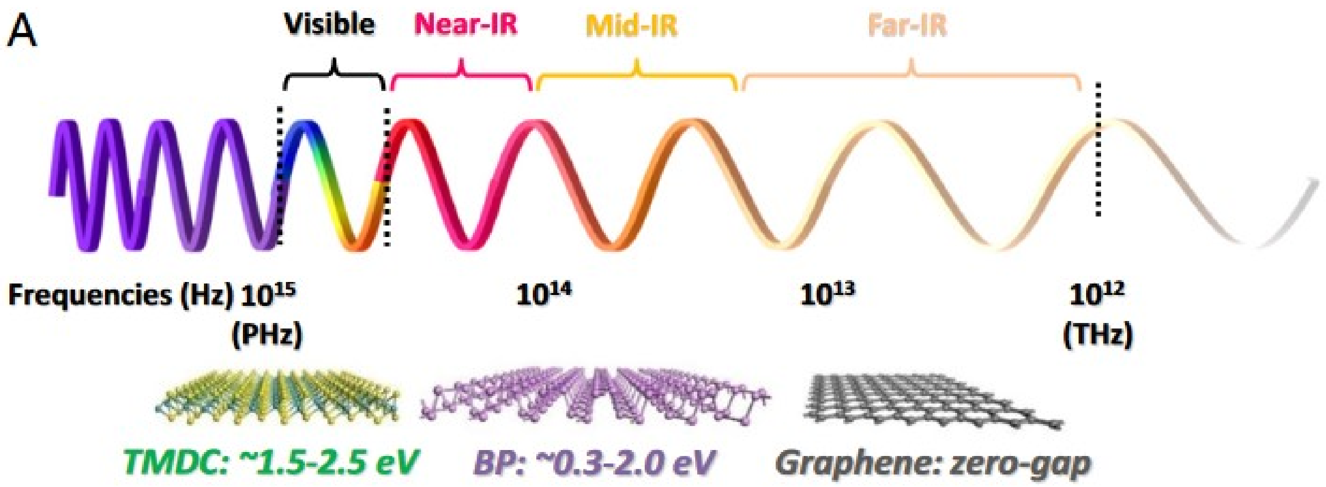


Chowdhury et al., Nature Nano. **4**, 235 (2009)

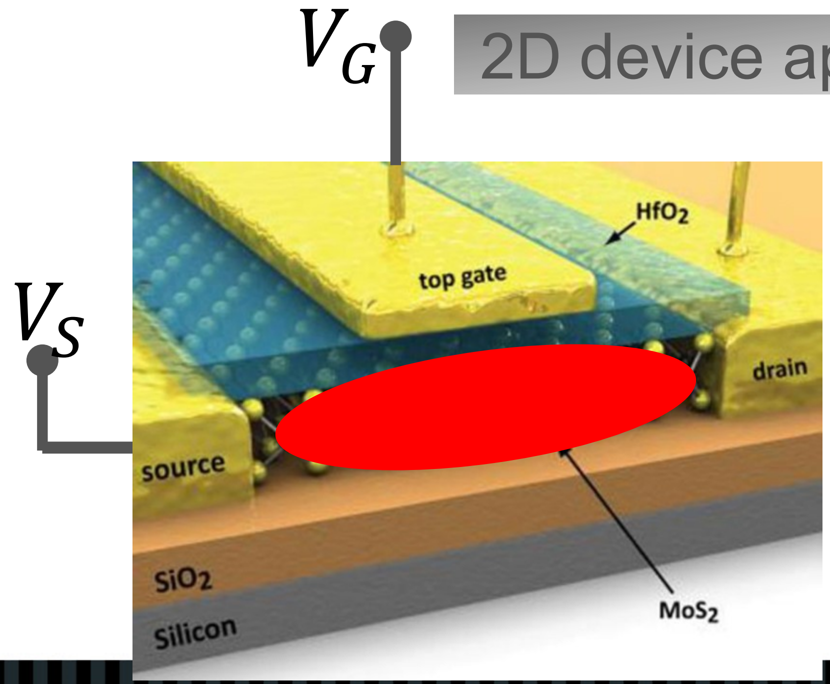
2D Materials "lasagna"

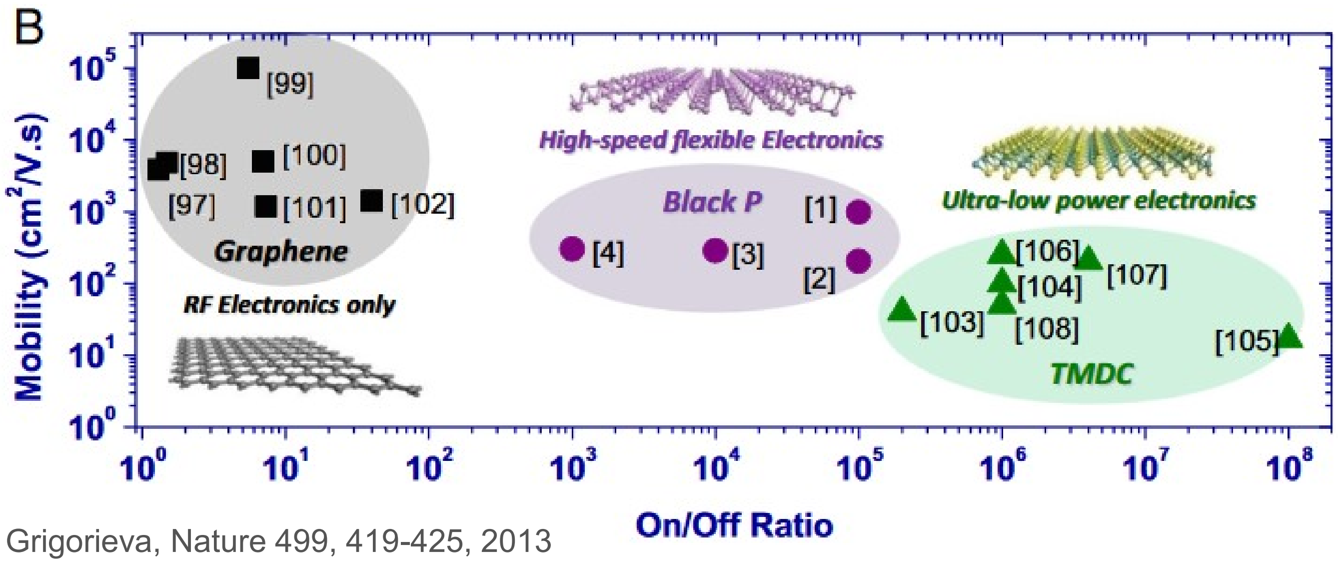


Optoelectronic applications



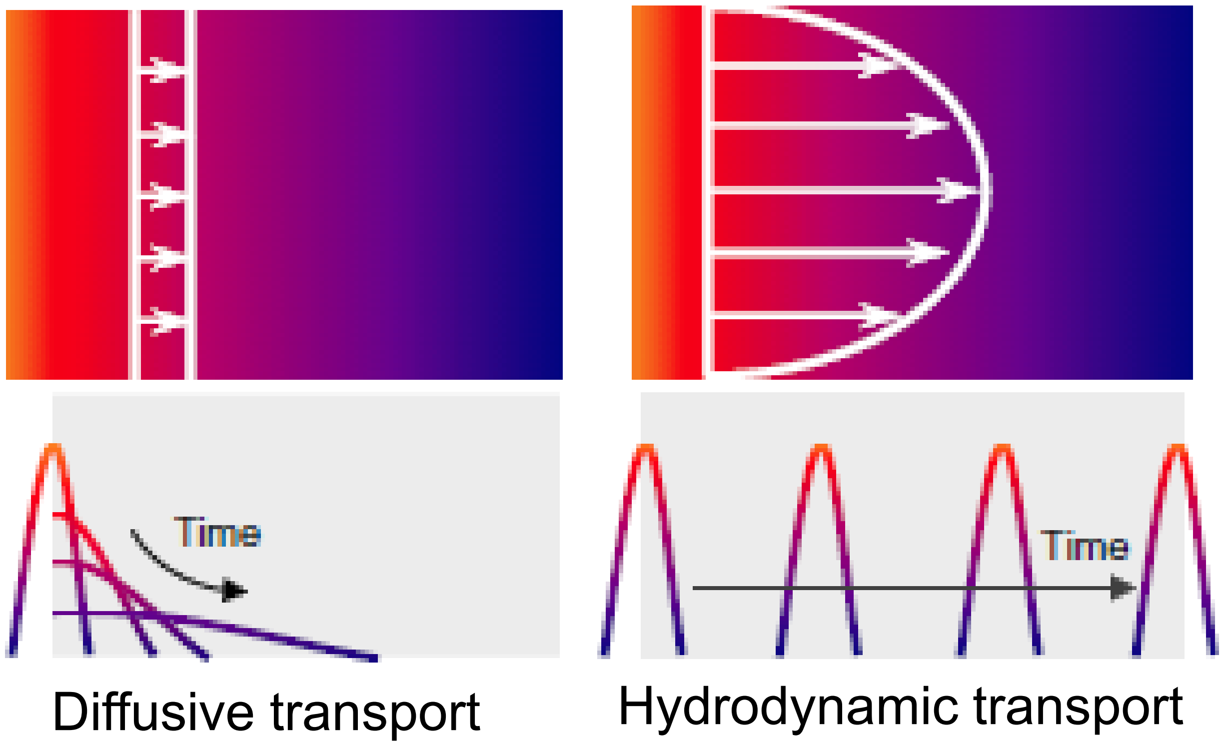
2D device applications



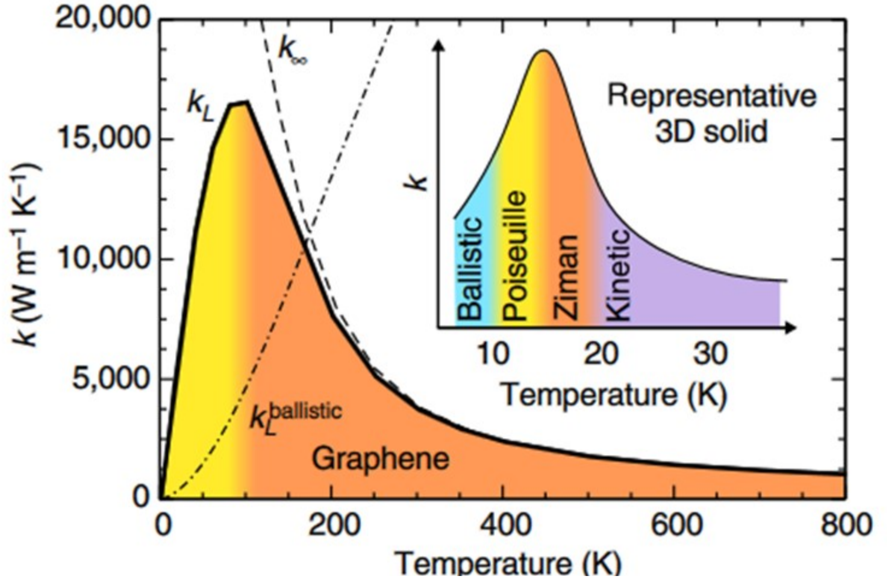


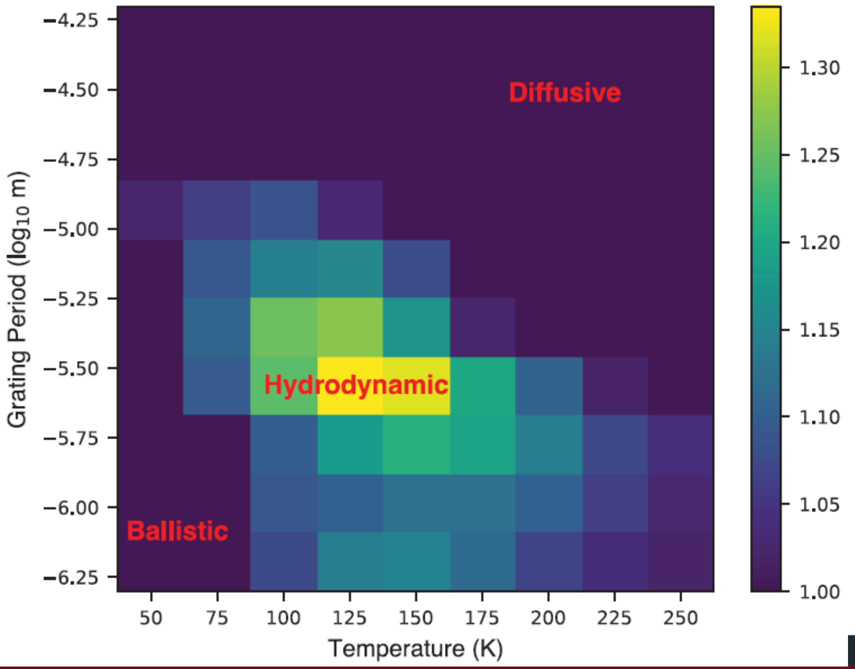
A.K. Geim and I.V. Grigorieva, Nature 499, 419-425, 2013
Ling et al., Proc. Nat. Acad. Sci. 112, 4523-4530 (2014)

Effective platform to take advantage of hydrodynamic (wave) transport of heat



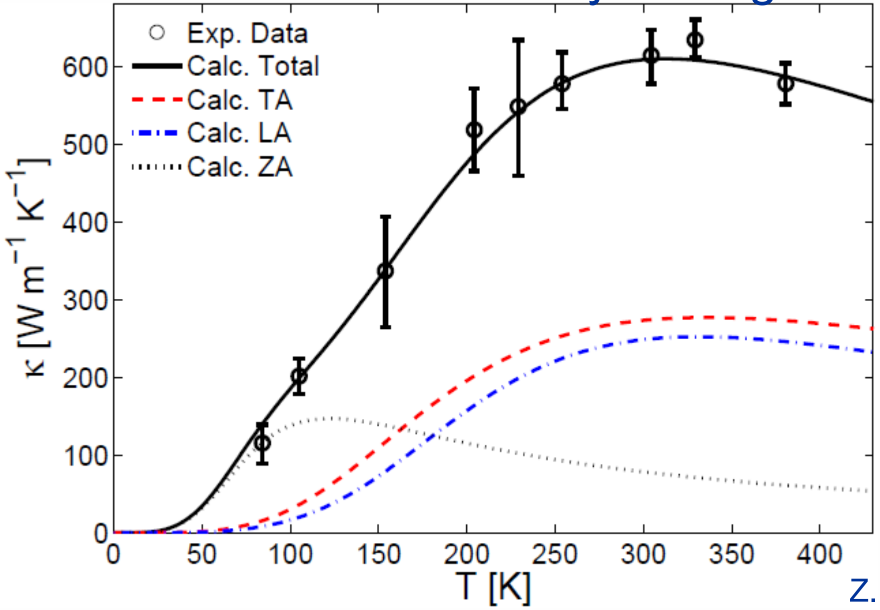
Lee et al., Nat. Commun. 6, 6290, 2015.
Cepellotti et al., Nat. Commun. 6, 6400, 2015.
Huberman et al., Science 364, 375–379, 2019.

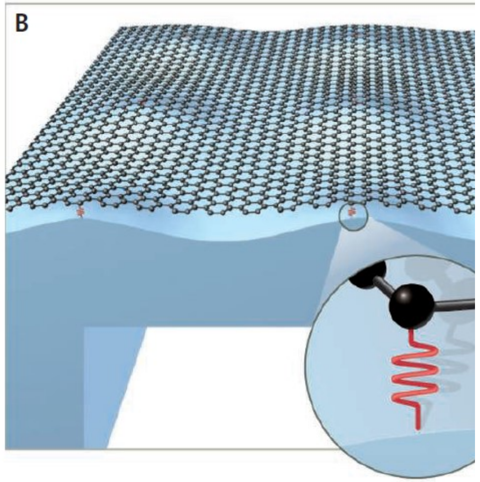


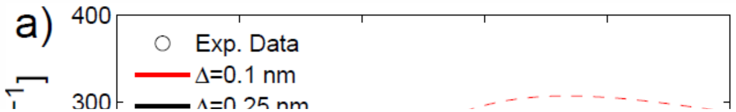


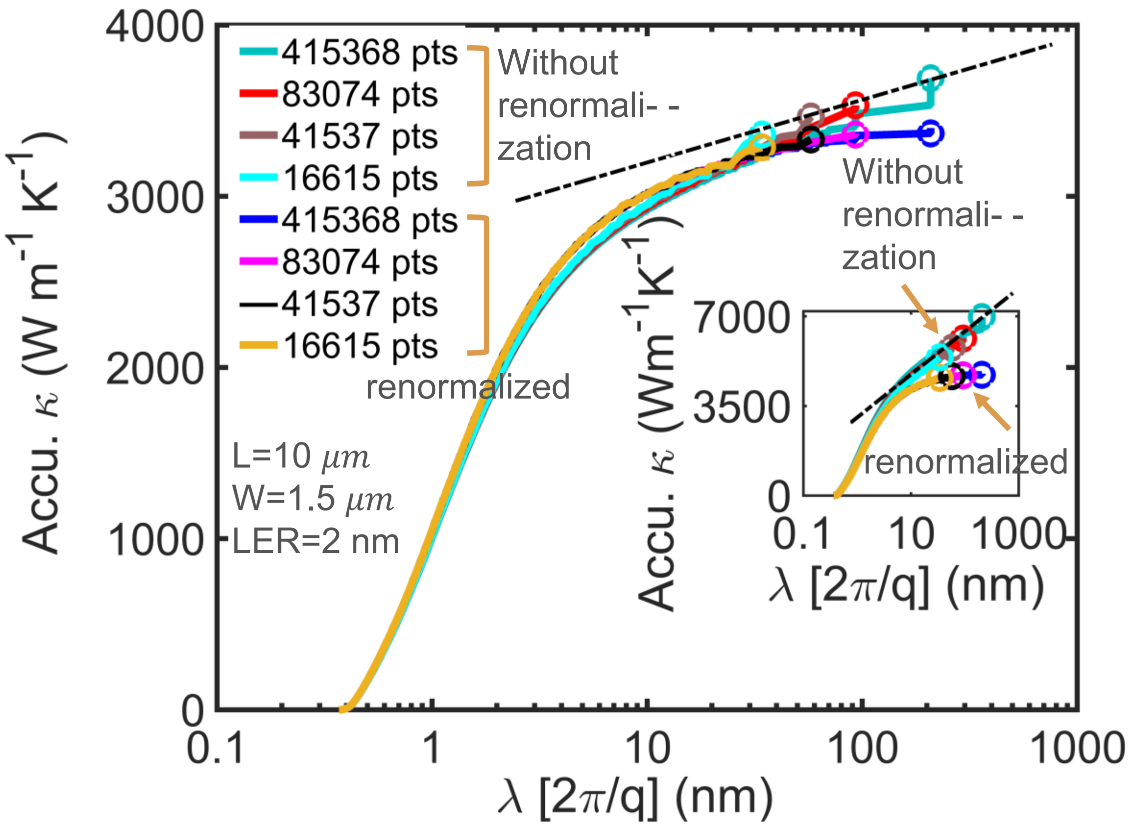
Thermal transport in supported graphene

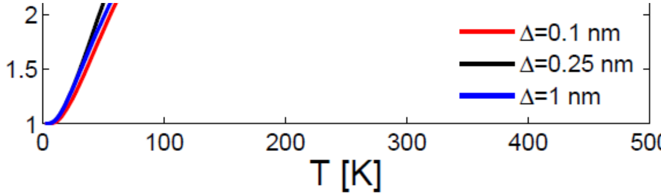
- Substrate scattering due to van der Waals interaction
- Drastic reduction in narrow supported GNR samples
- Thermal transport in narrow GNRs is highly anisotropic
- Thermal conductivity “diverges” with length up to 100 um











Z. Aksamija and I. Knezevic, Phys Rev. B,vol. 86, 165426 (2012).

Bae, Li, Aksamija, et al., Nature Comm. 4, 1734 (2013).

A.K. Majee and Z. Aksamija Phys. Rev. B 93, 235423, 2016

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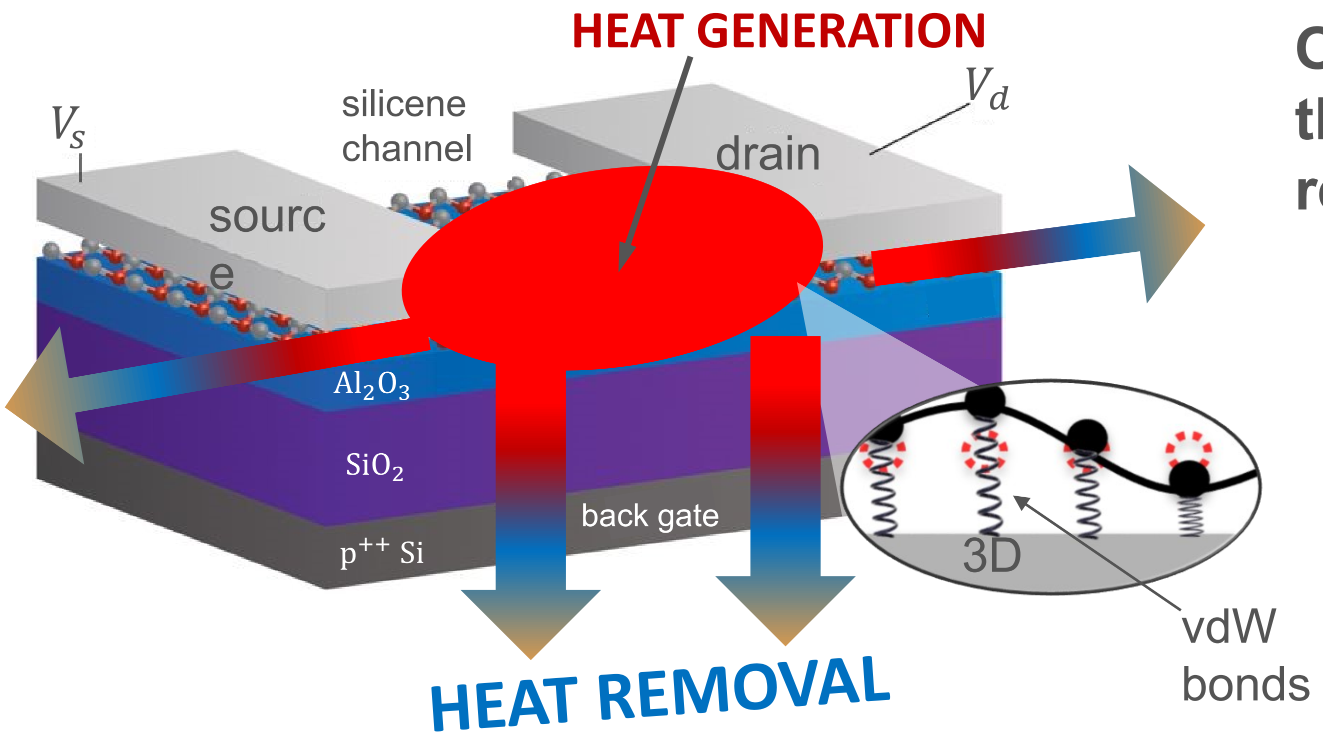
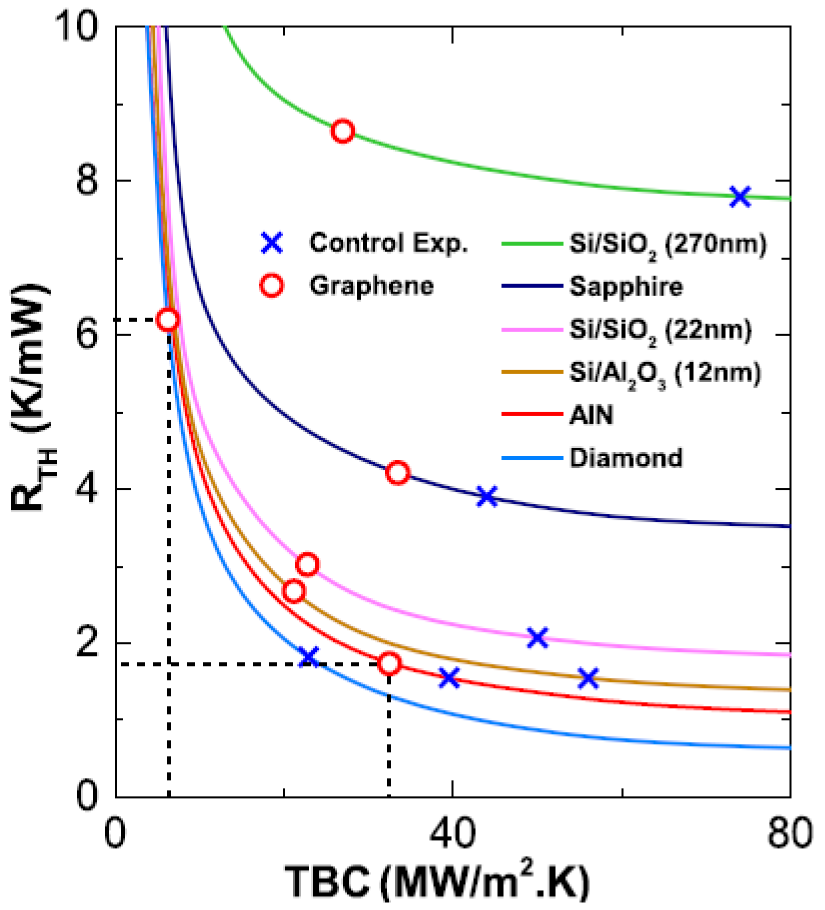
2D-3D thermal interface problem



Overall thermal resistance



2D-3D thermal interfaces pose significant concerns

- governed by **vdW** forces
- **sensitive** to approaches in synthesis
- essentially ***all interface***

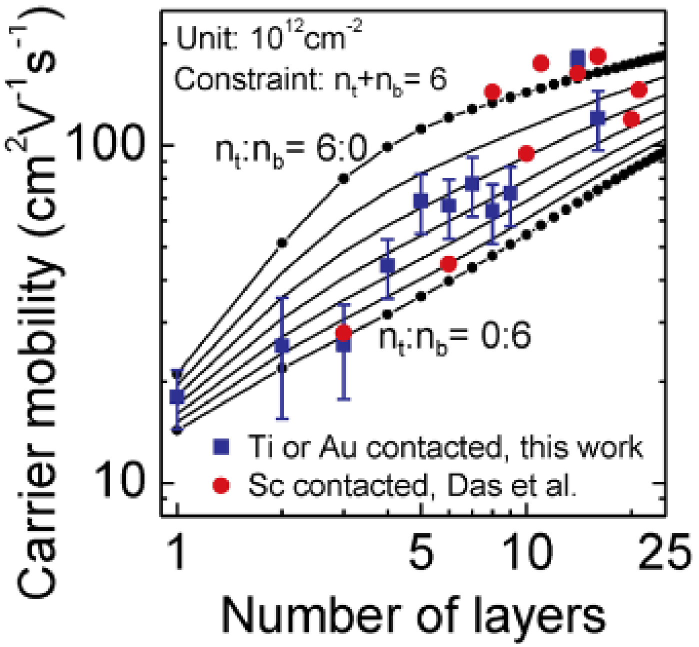
Most heat generated in a 2D device dissipates into the supporting substrate.

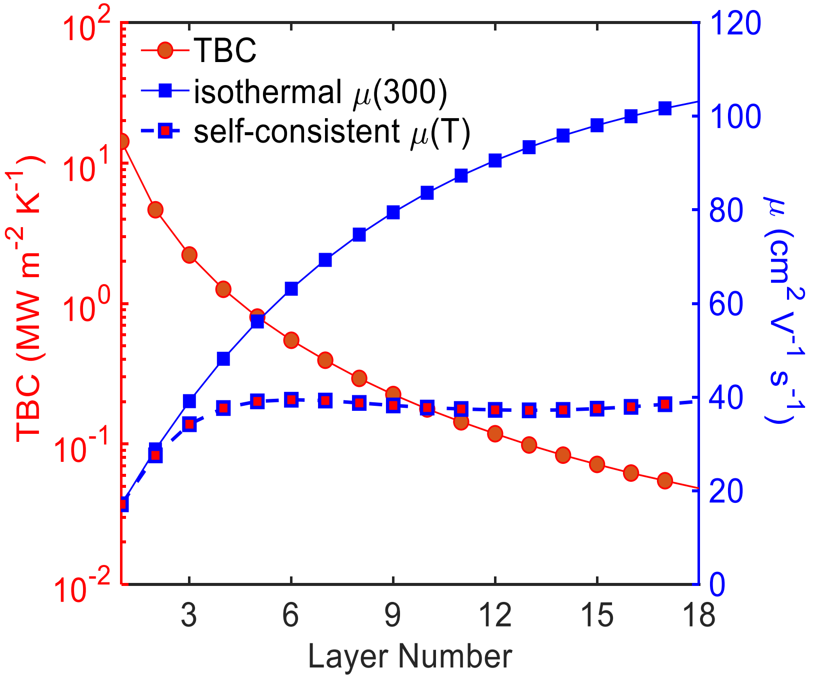
Hence, the thermal (2D/3D) interface formed strongly dictates the capabilities of thermal management in 2D devices.

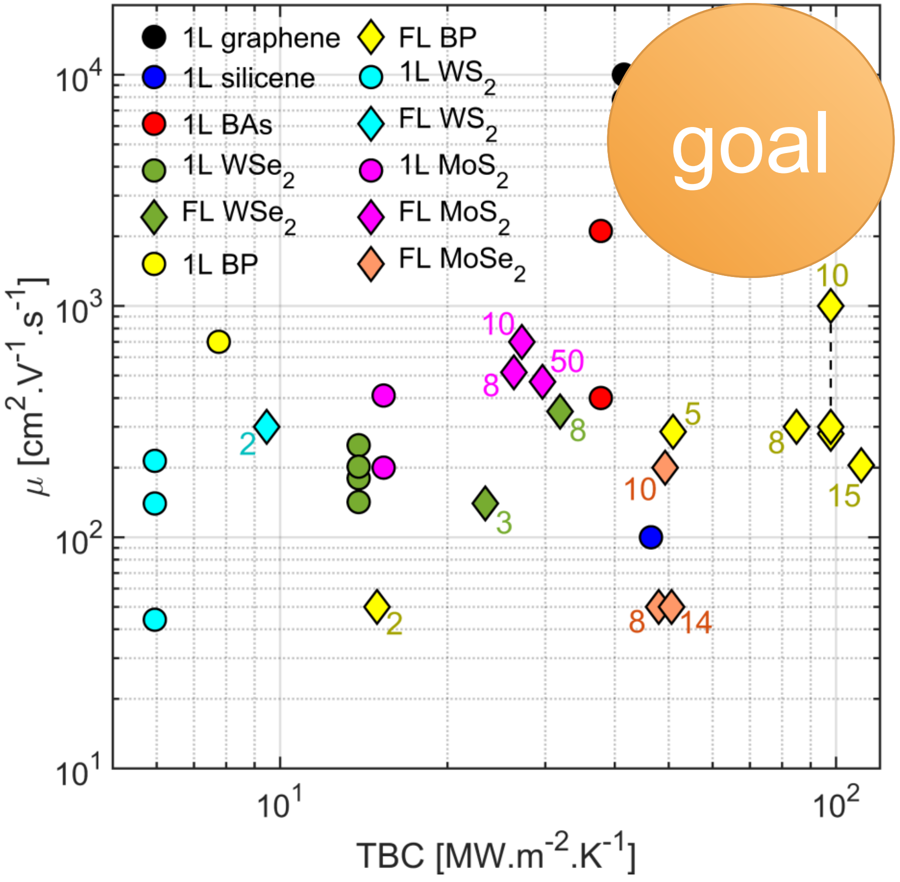
Nature Nano., vol. 6, p. 147–150, (2011).
Yasaei et al, *2D Mater.* 4 (2017) 035027

2D stacks for device applications

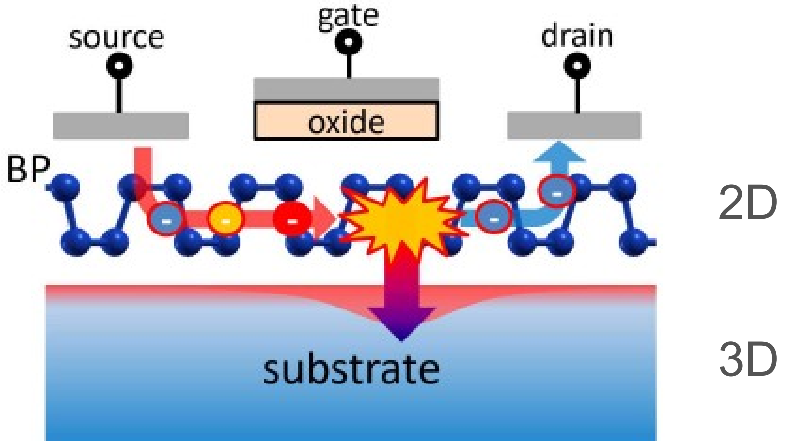
- Problem: self-heating degrades carrier mobility
- No 2D materials has simultaneously high mobility and thermal boundary conductance
- Mobility improves with thickness, which degrades thermal management

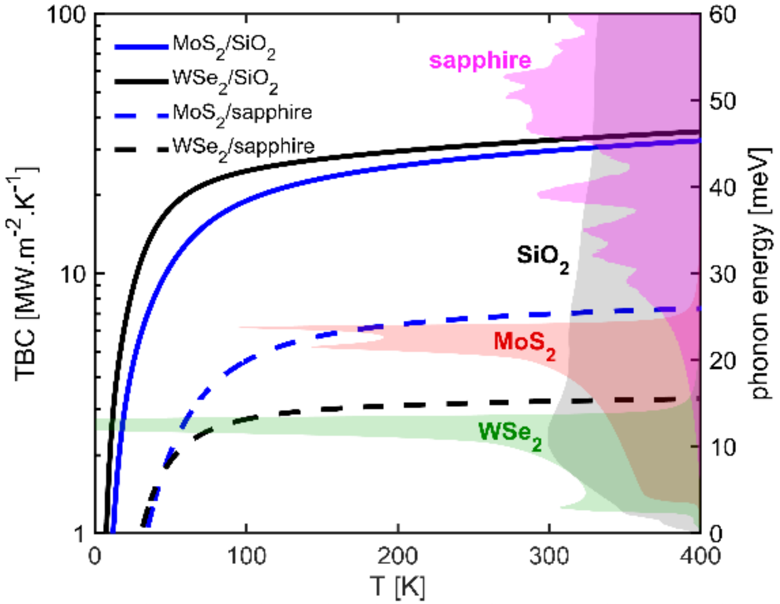


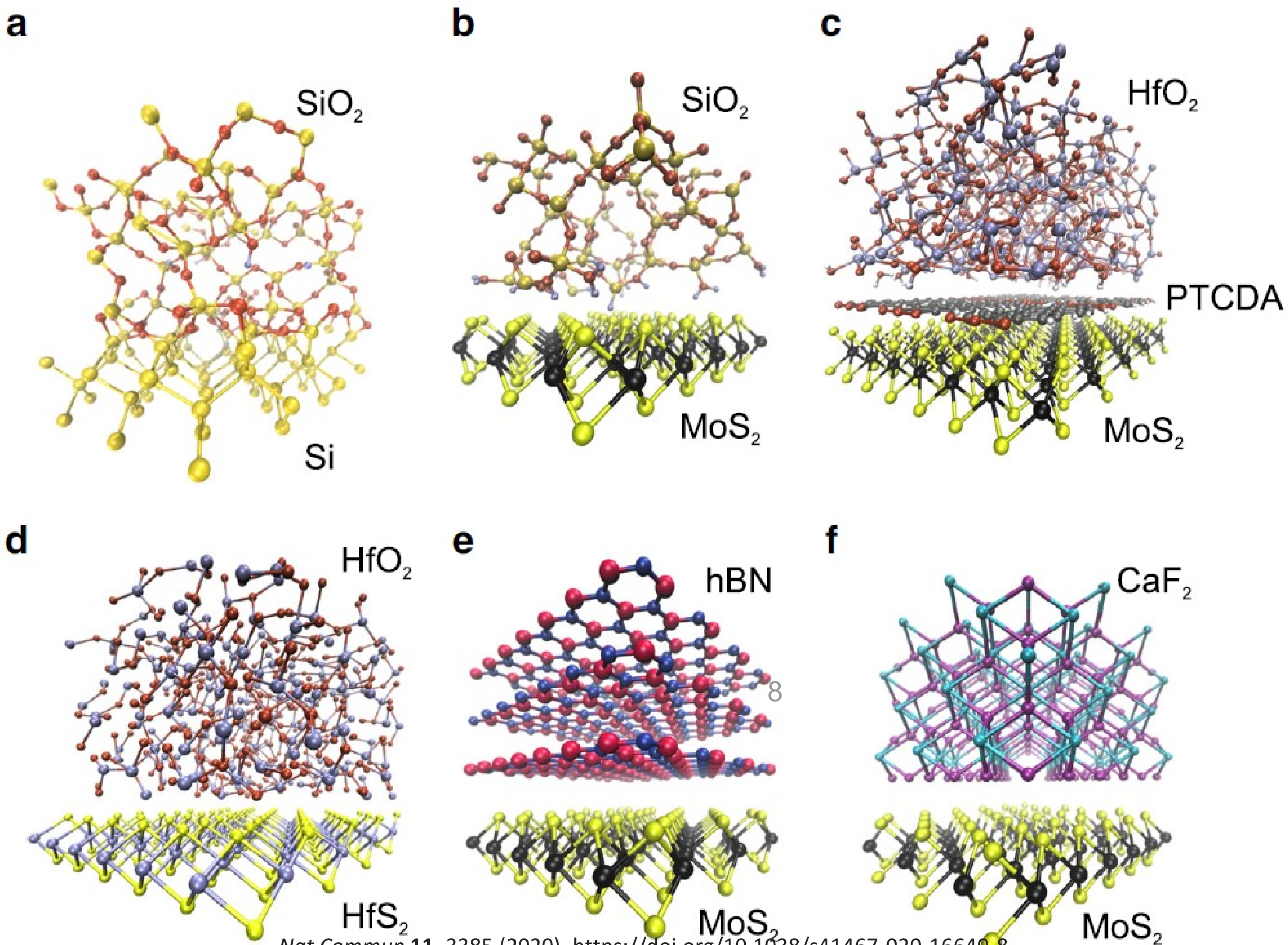




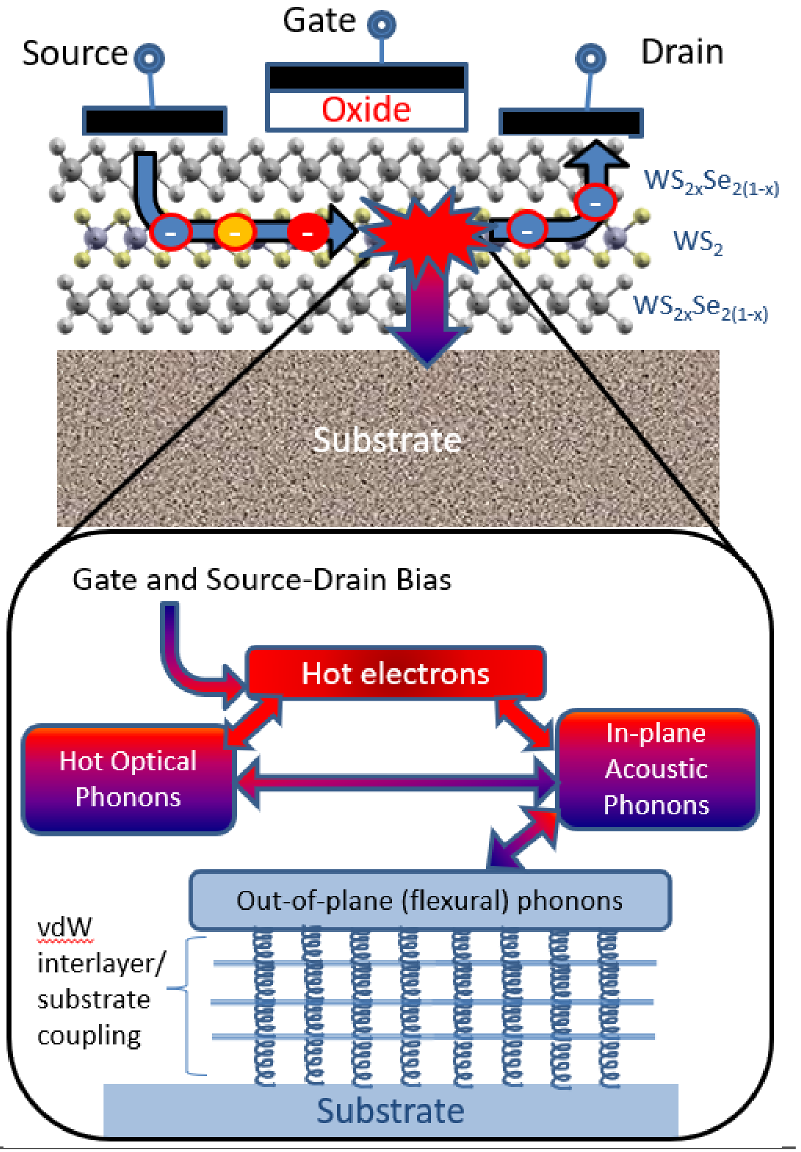
2D/3D Interface thermal resistance







Nat Commun **11,** 3385 (2020). https://doi.org/10.1038/s41467-020-16640-8

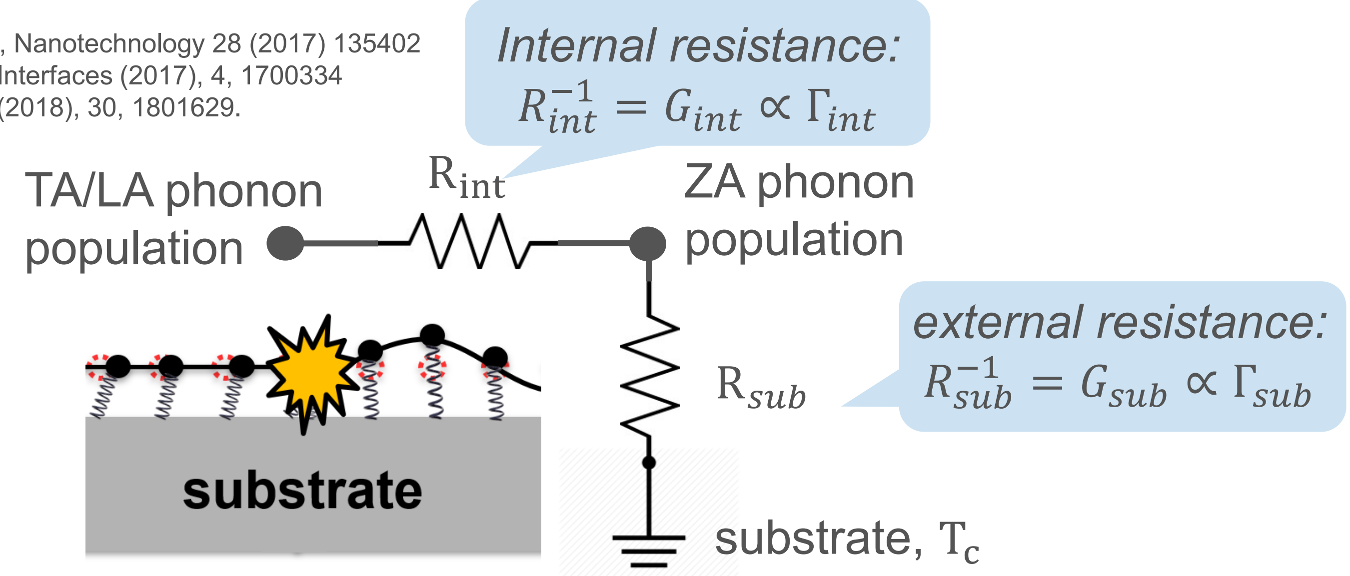


Flexural pathway of 2D-3D thermal transport

2D-3D TBC: $\Gamma_{TBC}(\omega)$

- weak van der Waals (vdW) bonding
- No cross-plane propagation ($v_g = 0$)
- Primary carrier of heat is ZA (flexural) phonons
- Scattering facilitates transport across the interface

Correa et al., Nanotechnology 28 (2017) 135402
Adv. Mater. Interfaces (2017), 4, 1700334
Adv. Mater. (2018), 30, 1801629.



IMAGINE THE UNIVERSITY OF UTAH

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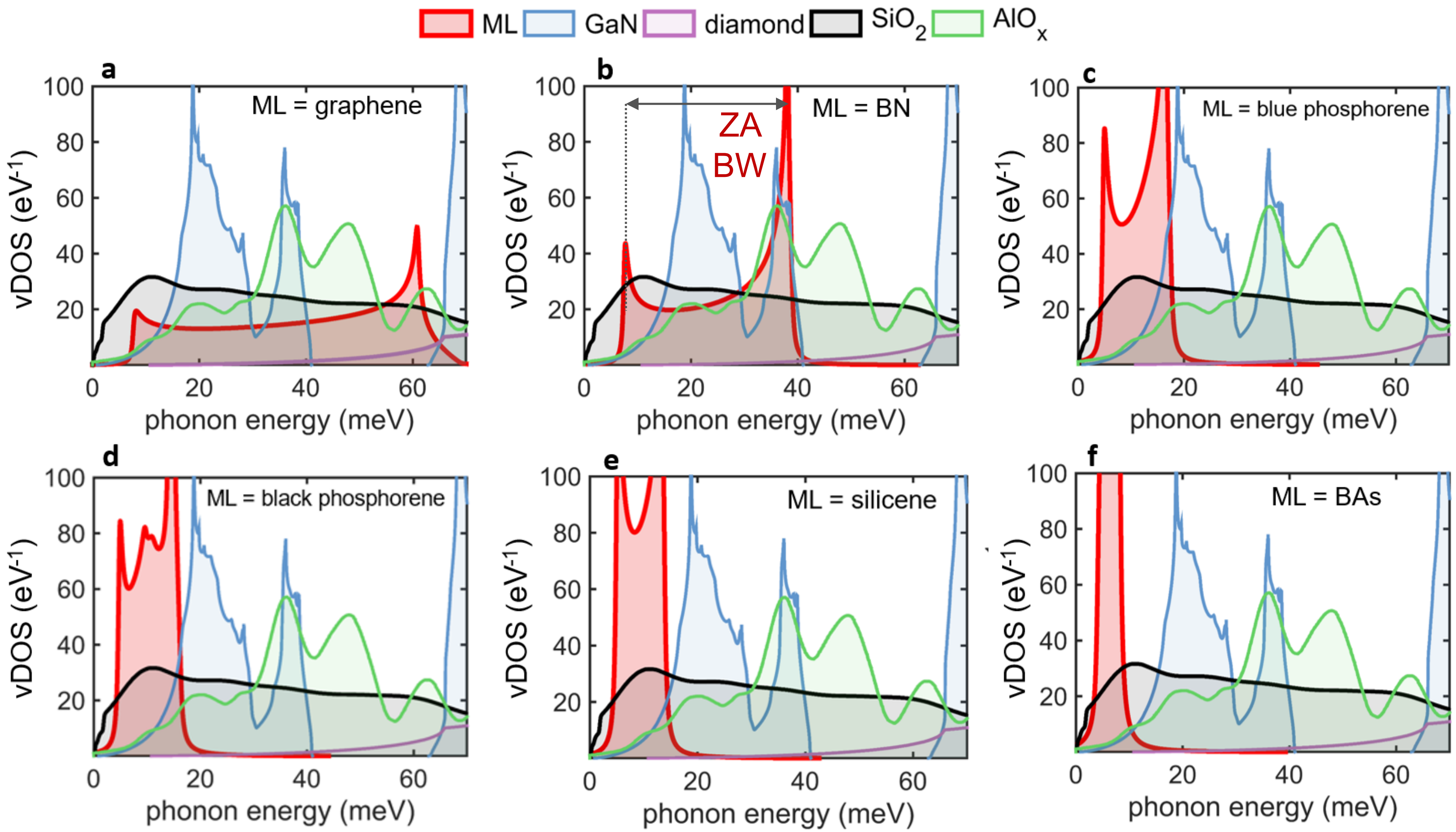

…at low energies!

Amorphous (boson peak):

$$D_{sub}(\omega) > \frac{\omega^2}{v_s^3}$$

Crystal (Debye):

$$D_{sub}(\omega) \propto \frac{\omega^2}{v_s^3}$$

$$G_{ext}(T) \propto D_{2D} D_{sub}$$

$$\Gamma_{sub} \propto \frac{1}{\omega^2}$$

ML=monolayer
BW=bandwidth

External TBC strongly depends on DOS overlap.
A narrower ZA bandwidth should lend itself to a larger external TBC.

Cameron J Foss and Zlatan Aksamija
2019 *2D Mater.* **6** 025019

TBC of 2D-crystalline interfaces

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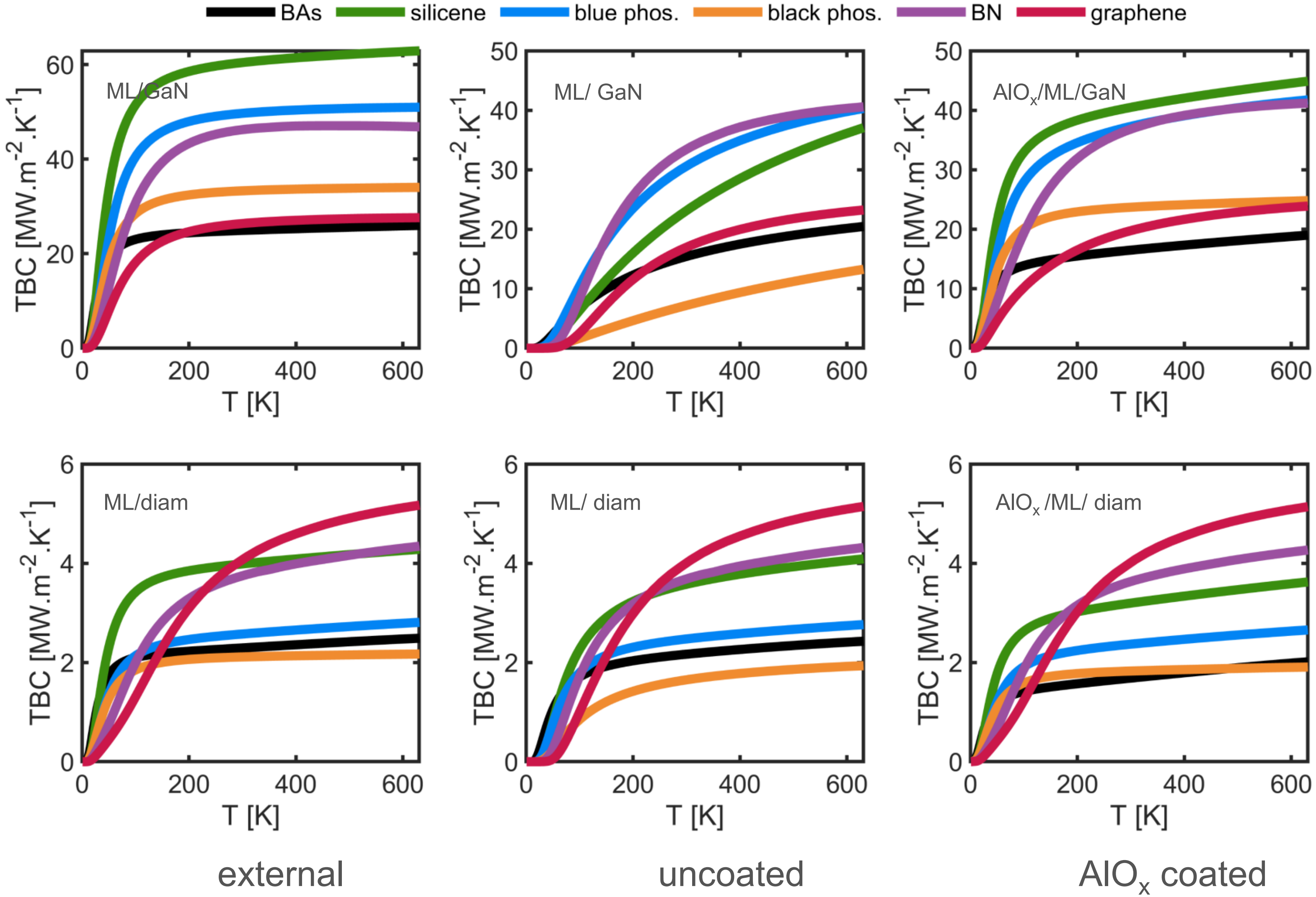

On crystals with high sound velocity (i.e., small low energy vDOS) like diamond, 2D materials with broader ZA BWs are preferred such as graphene and BN.

$$\Gamma_{sub} \propto \frac{1}{\omega^2}$$

Cameron Foss and Zlatan Aksamija
2021 *Nanotechnology* **32** 405206

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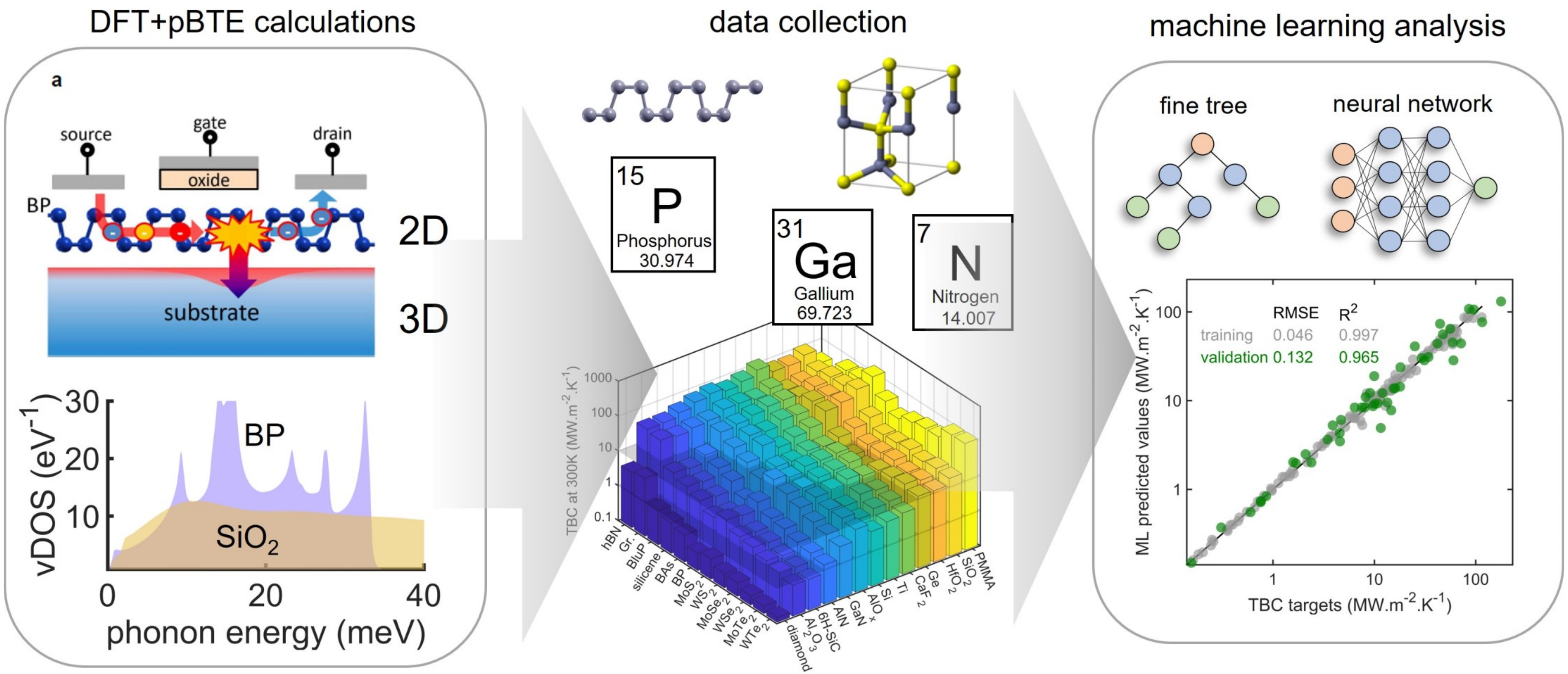
Machine learning model for 2D/3D TBC



Goal(s): Develop a streamlined predictive model that can be used to suggest ultrahigh/low TBC pairings and distill the most impactful material descriptors from our theoretical model using sensitivity analysis.

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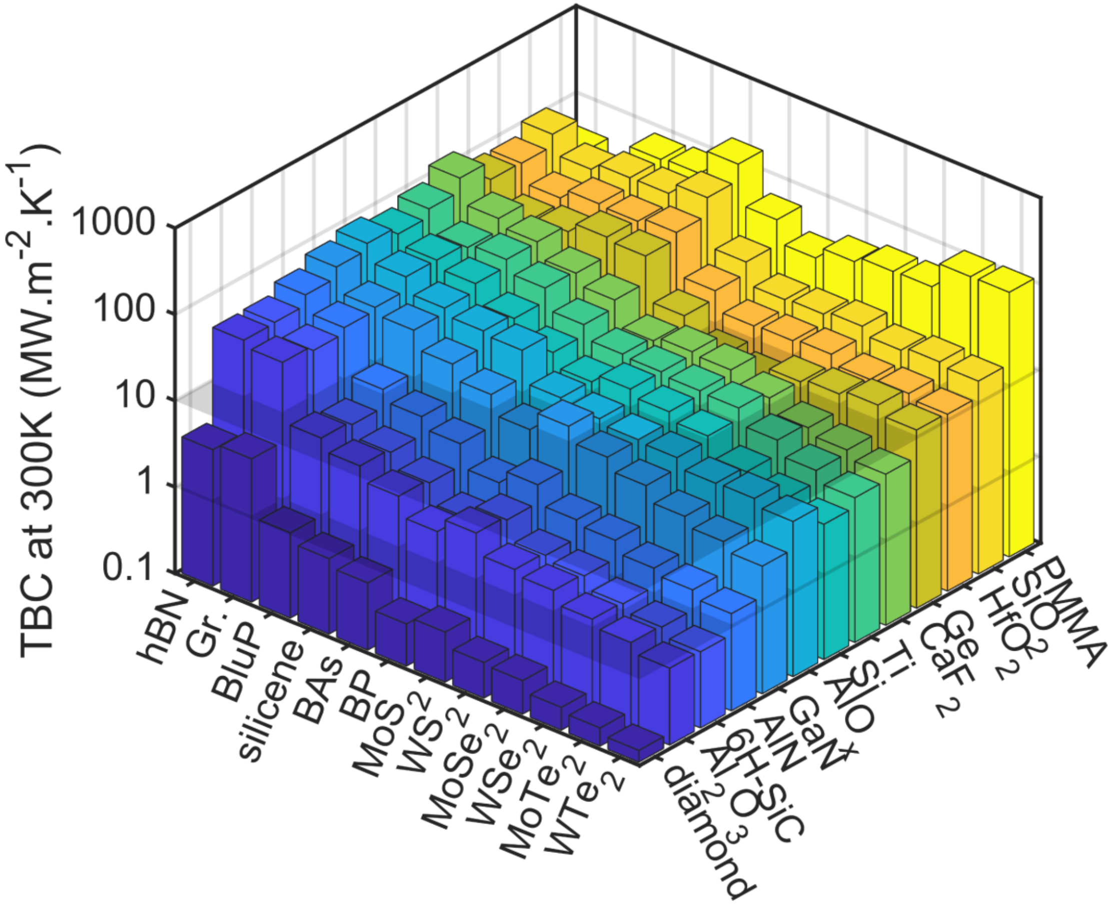
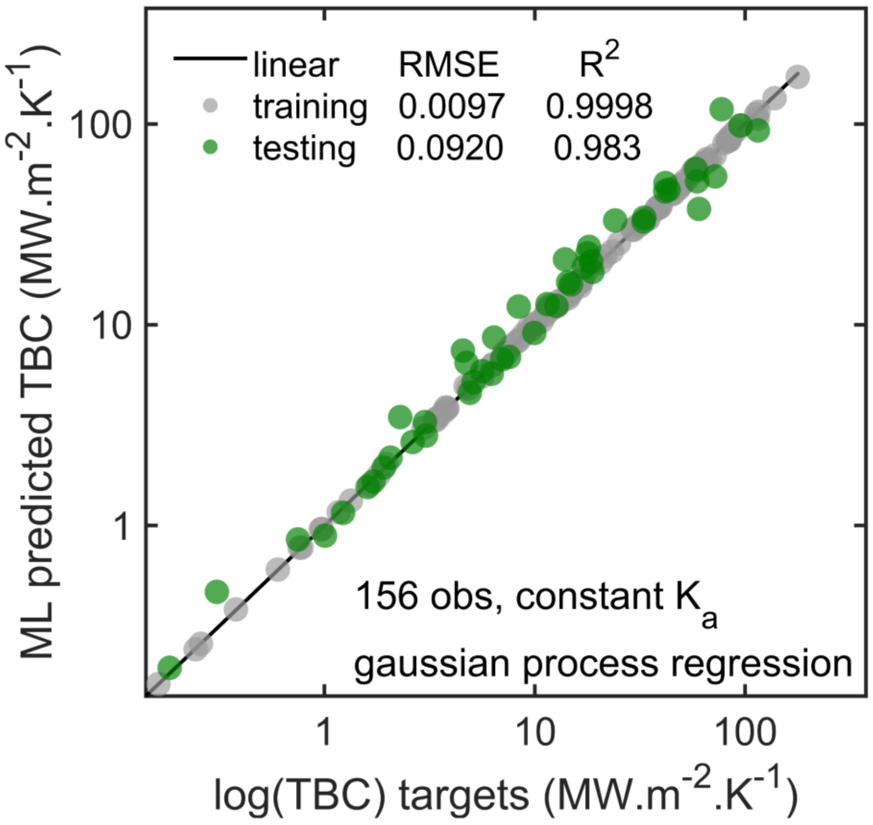
Results: room-temperature TBC and ML fitting





- Best performing pairs are BAs/PMMA, hBN/CaF_2, and BAs/SiO_2 (100-150 $MW.m^{-2}.K^{-1}$)
- Worst performing substrates are diamond, Al_2O_3, and 6H-SiC (<10 $MW.m^{-2}.K^{-1}$)
- Paper: Foss and Aksamija, Appl. Phys. Lett. 122, 062201 (2023), Data: https://nanoenergy.mse.utah.edu/codesdata/

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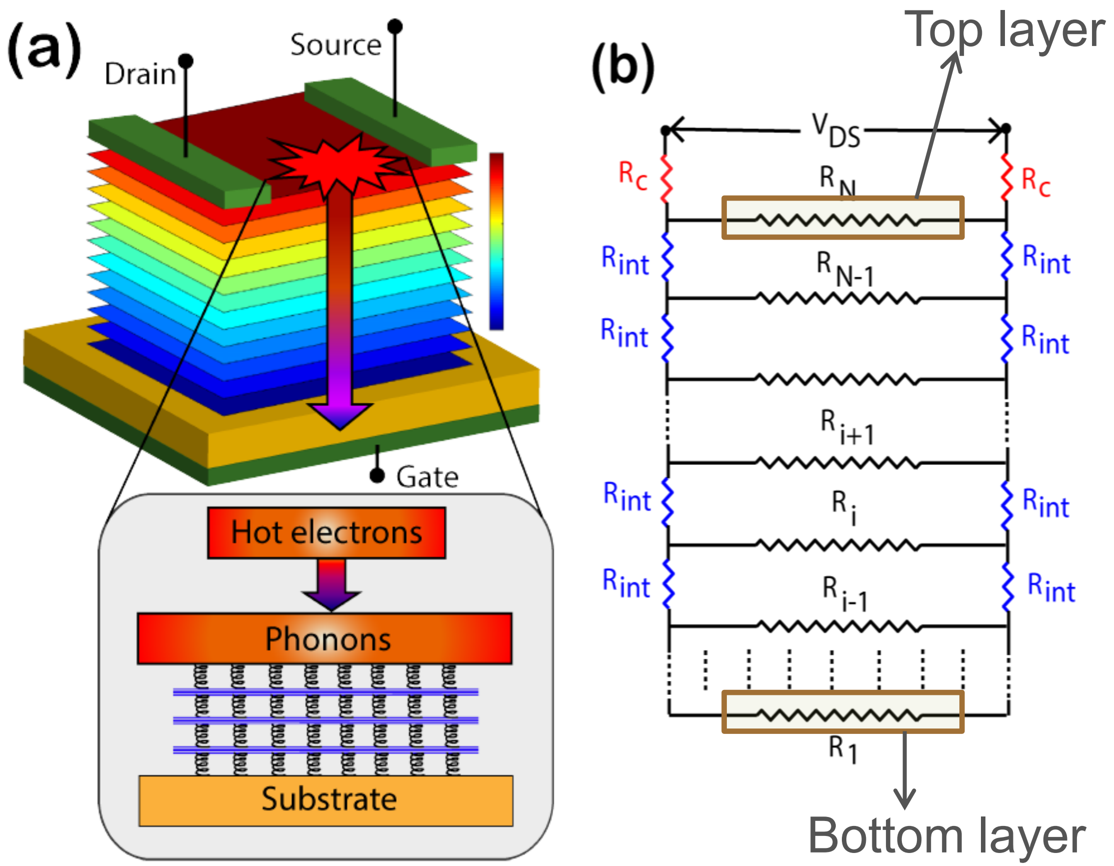
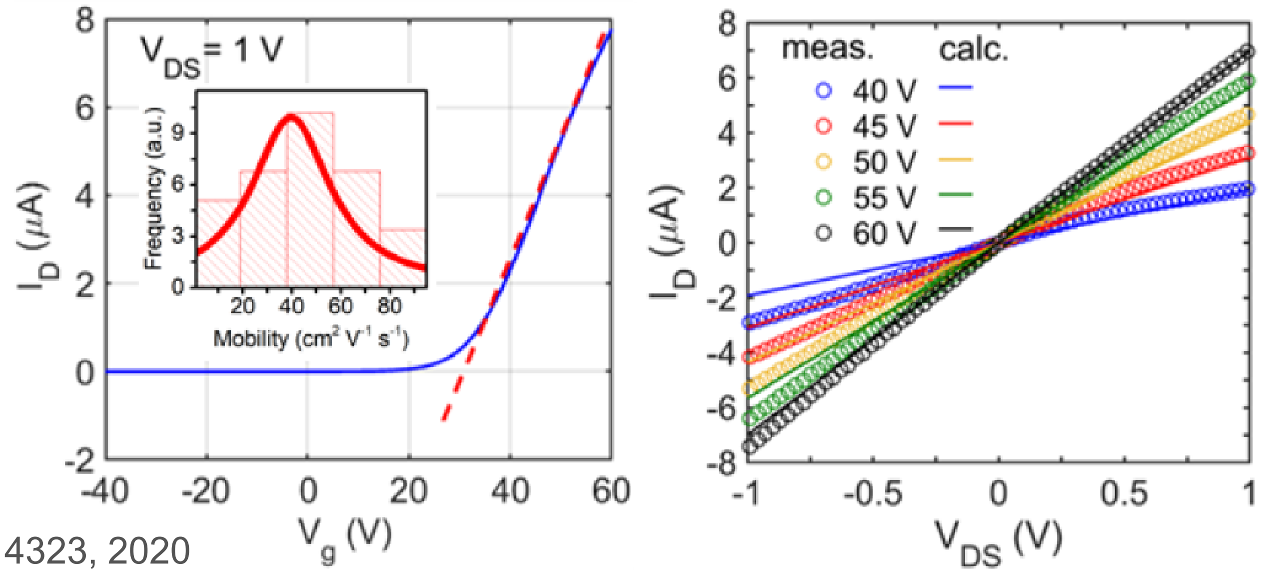
Dissipation and self-heating in 2D WSe_2 devices



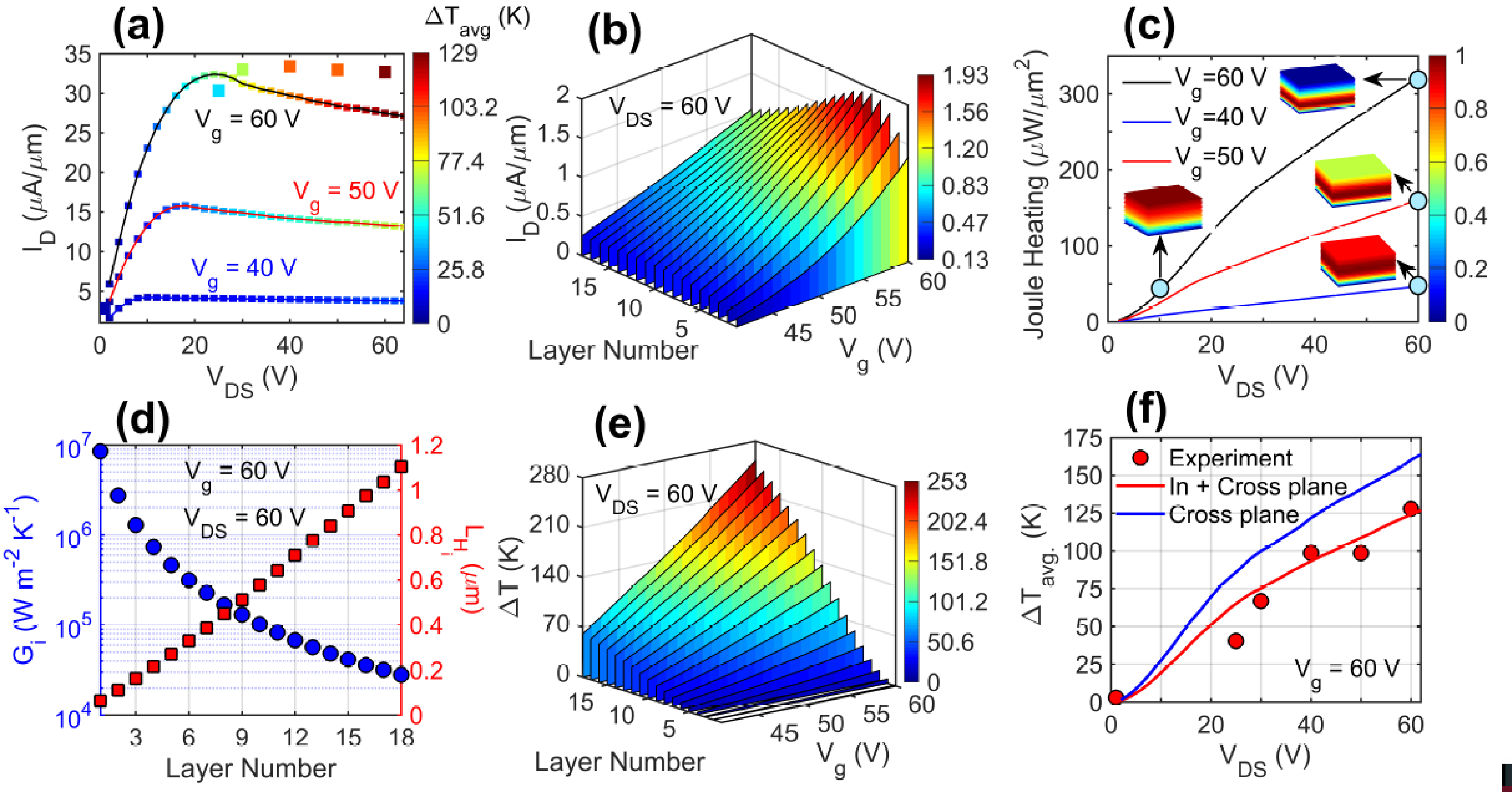
- Few-layered 2D devices offer higher mobility and current carrying capacity
- Current flow and heat dissipation are not uniform
- We characterized and simulated an 18-layer WSe_2 FET
- Raman measurements quantify temperature
- Significant self-heating leads to mobility degradation



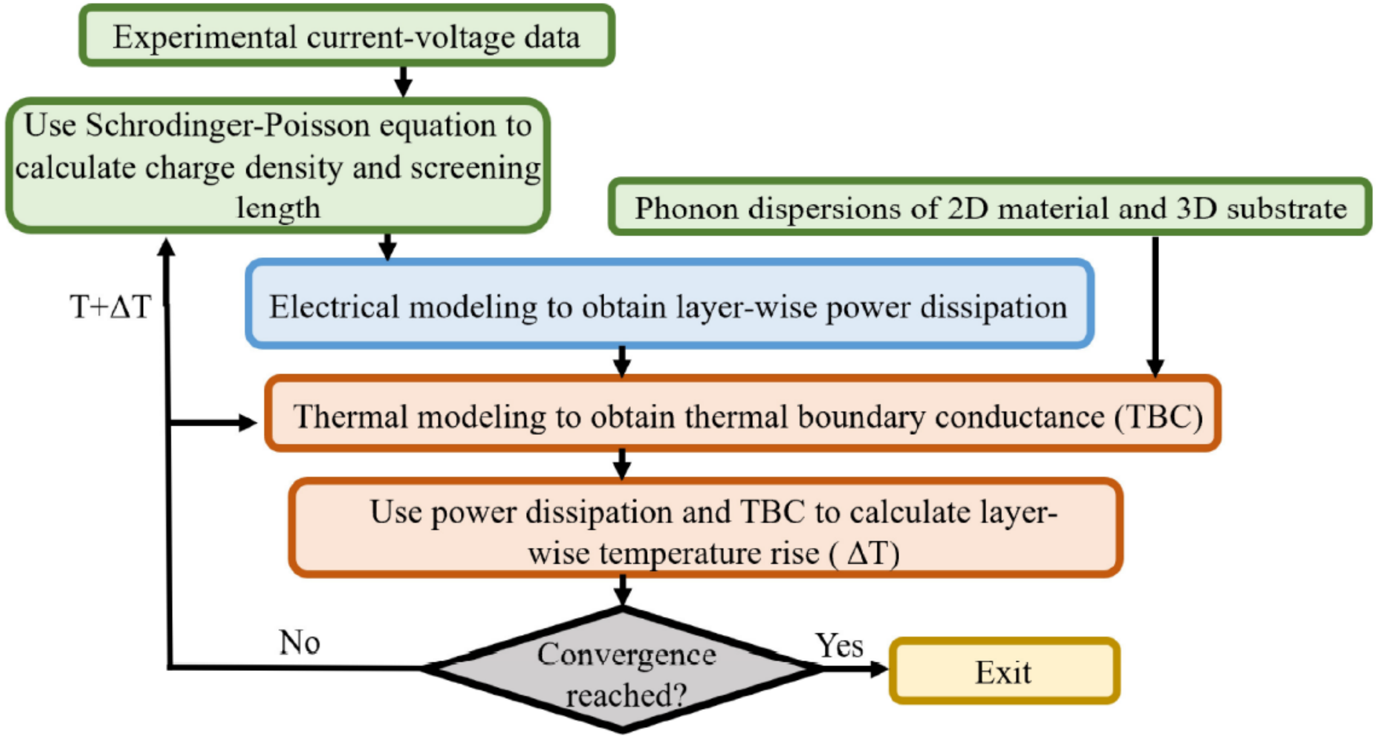
Initial model: Das and Appenzeller, Nano Lett. 2013, 13, 7, 3396–3402

Our model+experiments: Majee et al., ACS Appl. Mater. Interfaces 20, 14323, 2020

Novel current re-routing mechanism

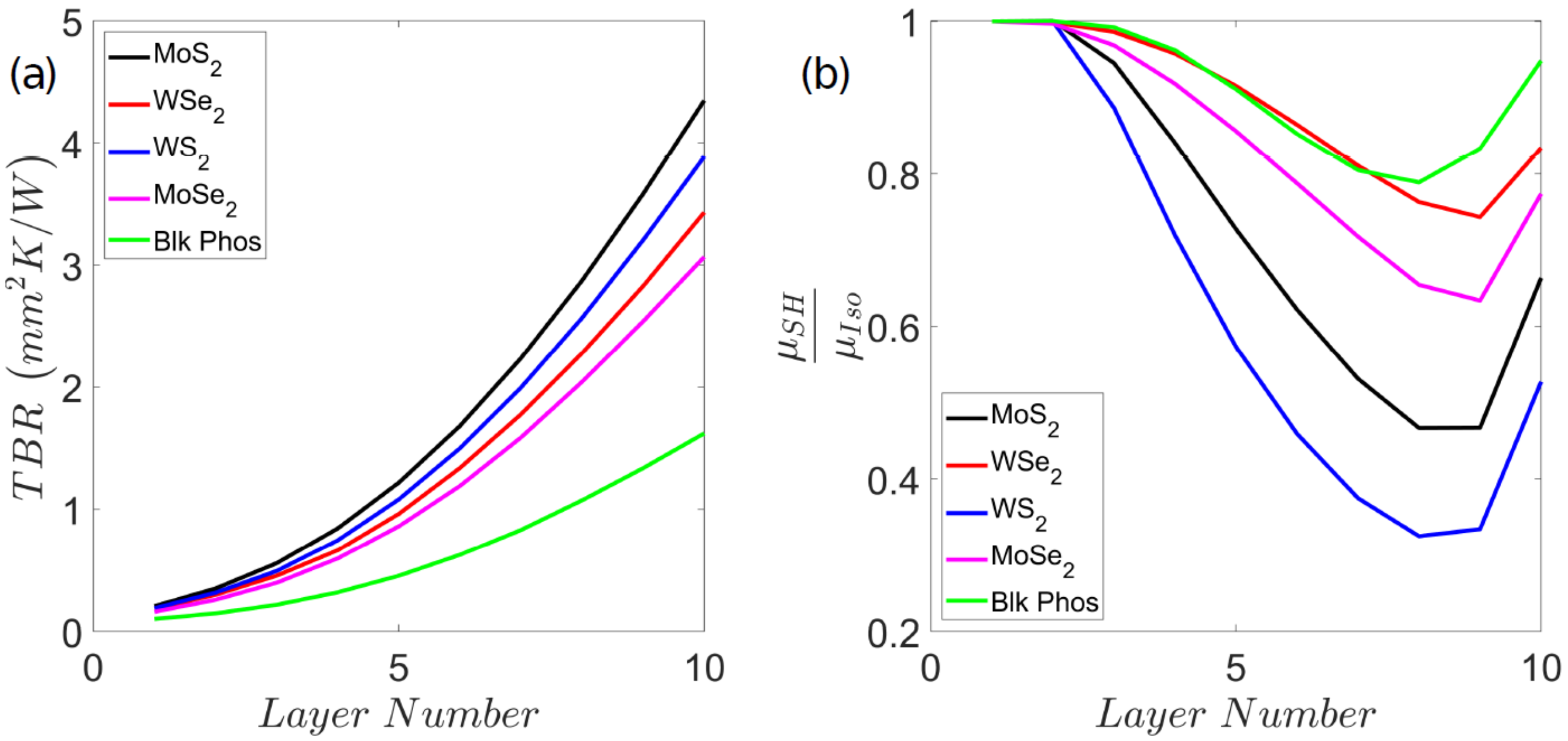


Adding self-consistent Schroedinger-Poisson



- Solve the coupled Schroedinger-Poisson in the vertical (through-plane) direction at every "slice" along channel
- Wrap the self-consistent electro-thermal loop around the electron transport model
- Each layer has a temperature-dependent mobility, Joule heating, and effective thermal conductance

Mobility degradation for 10-layer stacks



- We compare mobility degradation due to self-heating across the 4 canonical TMDs and BP
- BP has the highest TBC (lowest TBR), resulting in the lowest mobility degradation

Conclusions

- Heat dissipation a crucial bottleneck to 2D devices
- Heat transfer primarily via vdW bonds to substrate
- Exacerbated in 2D stacks: added interlayer thermal resistance
- Matching 2D layer to 3D substrate controls TBC
- Machine Learning to predict ideal 2D-substrate pairings
- Coupled electro-thermal model to identify best performing materials

- QUESTIONS? zlatan.aksamija@utah.edu