Compact modeling of memristors for neuromorphic circuit simulation

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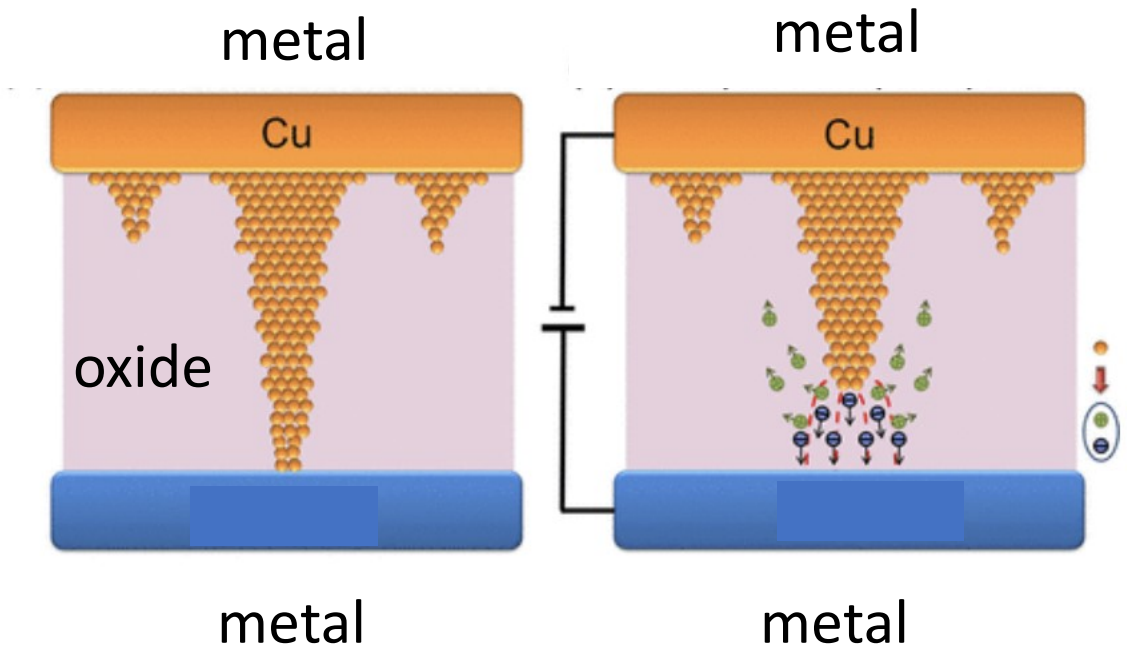
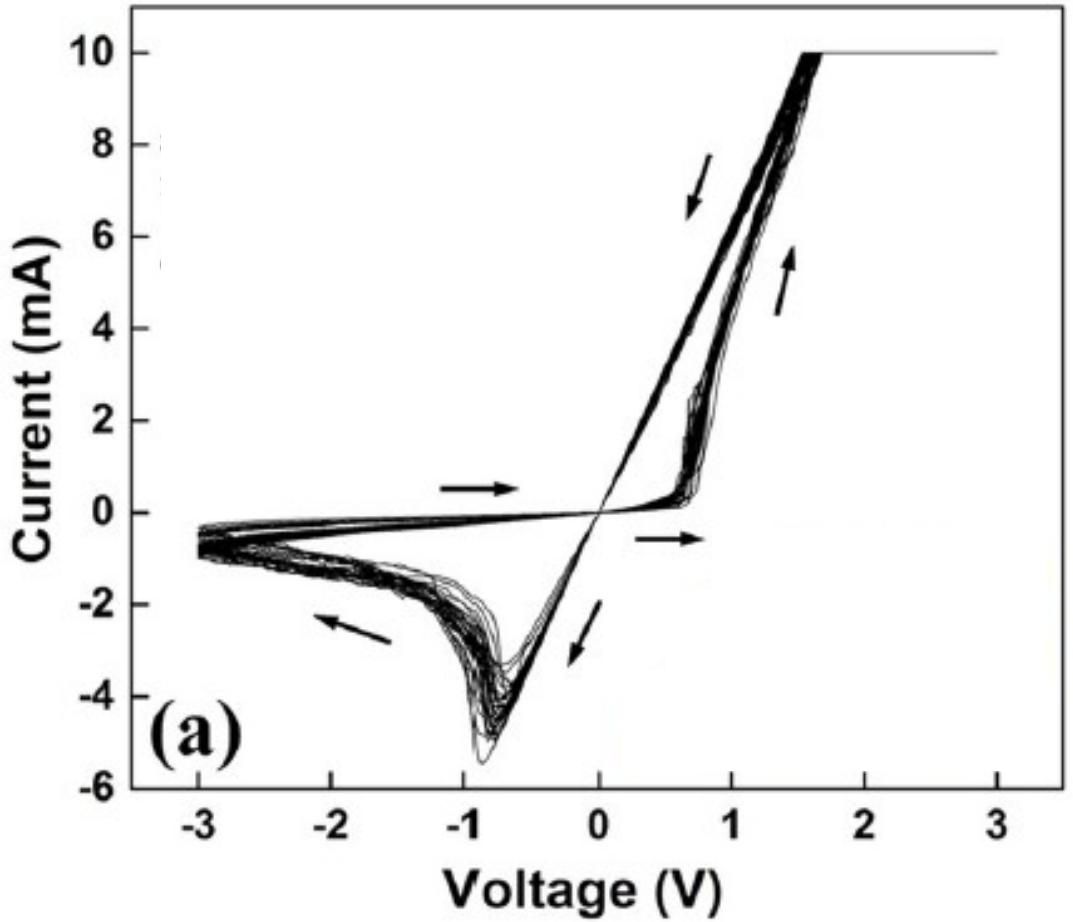
Memristive devices





- Non-volatile memories
- Neuromorphic circuits
  (beyond Von Neumann analog in-memory computing)

Compact models

- **Full physical models** are required to understand and design devices with the required properties **but** are useless for circuit simulation

- **A compact model** provides a simple description of the device electrical properties with the goal of circuit simulation

- Here we deal with a “physics-inspired” behavioural model

Modeling electro-ionic devices

Ions change the shape of the conducting filament and the **memory state**.

STATE EQUATION

λ

Electron injection determines the **I-V characteristics**.

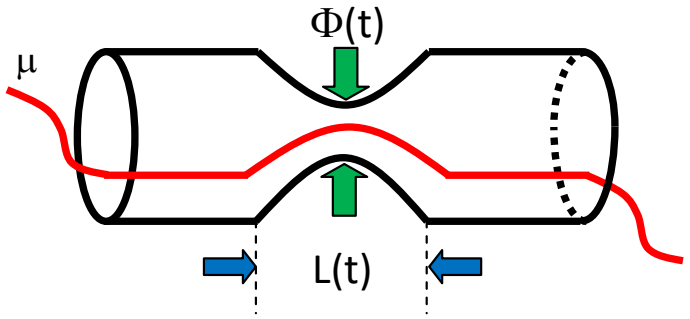
$I_0 = I_0(\lambda)$

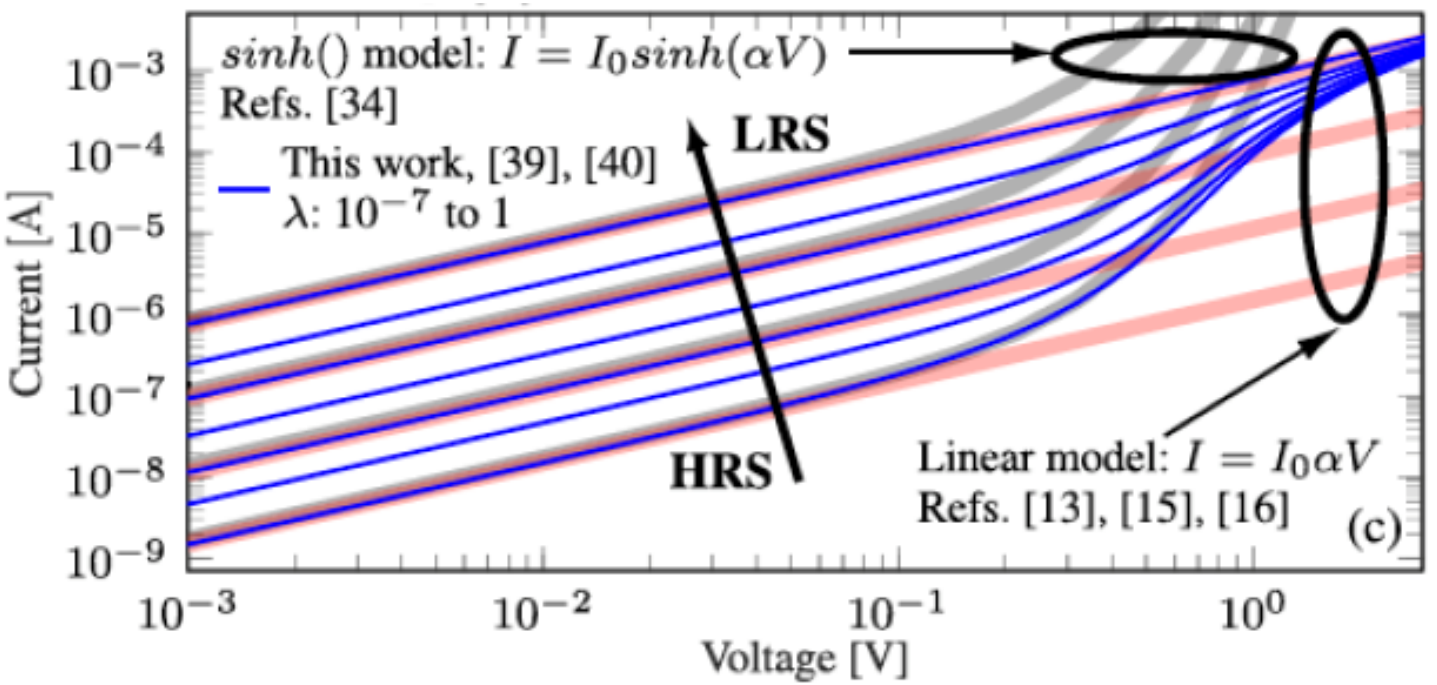
CURRENT EQUATION

$$I_0(\lambda) = (I_{0max} - I_{0min})\lambda + I_{0min}$$

E. Miranda and J. Suñé, *IEEE Transactions on Nanotechnology*, 19, 837, (2020)

Current equation





$$I_0 = I_0(\lambda)$$

$$I(V_C) = I_0 sinh[\alpha(V_C - R_S I)]$$

Memory equation

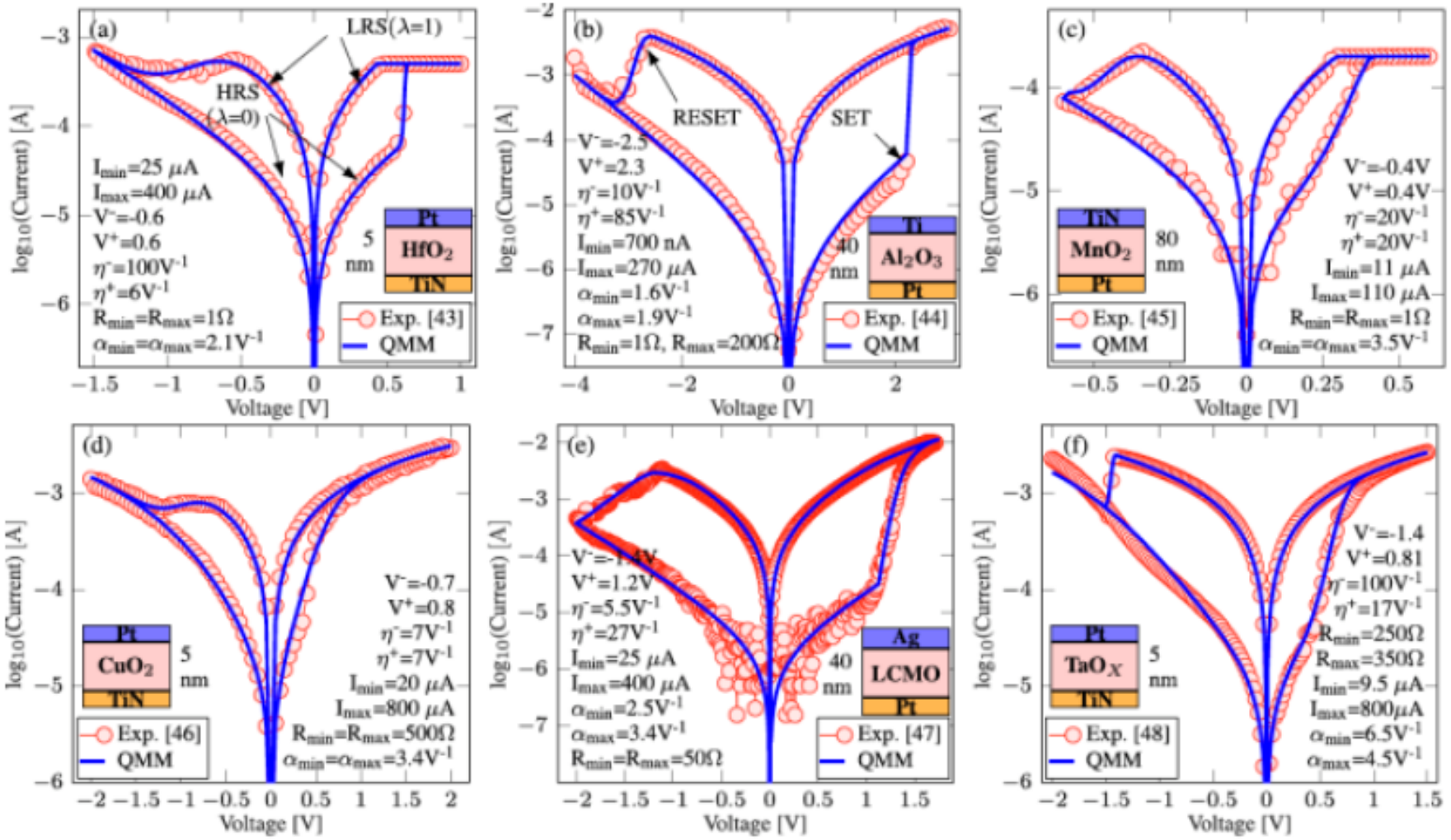
$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda, V_C)} - \frac{\lambda}{\tau_R(\lambda, V_C)}$$

$$\tau_{S,R}(V) = \exp\left[-\eta_{S,R}\left(V - V_{S,R}\right)\right]$$

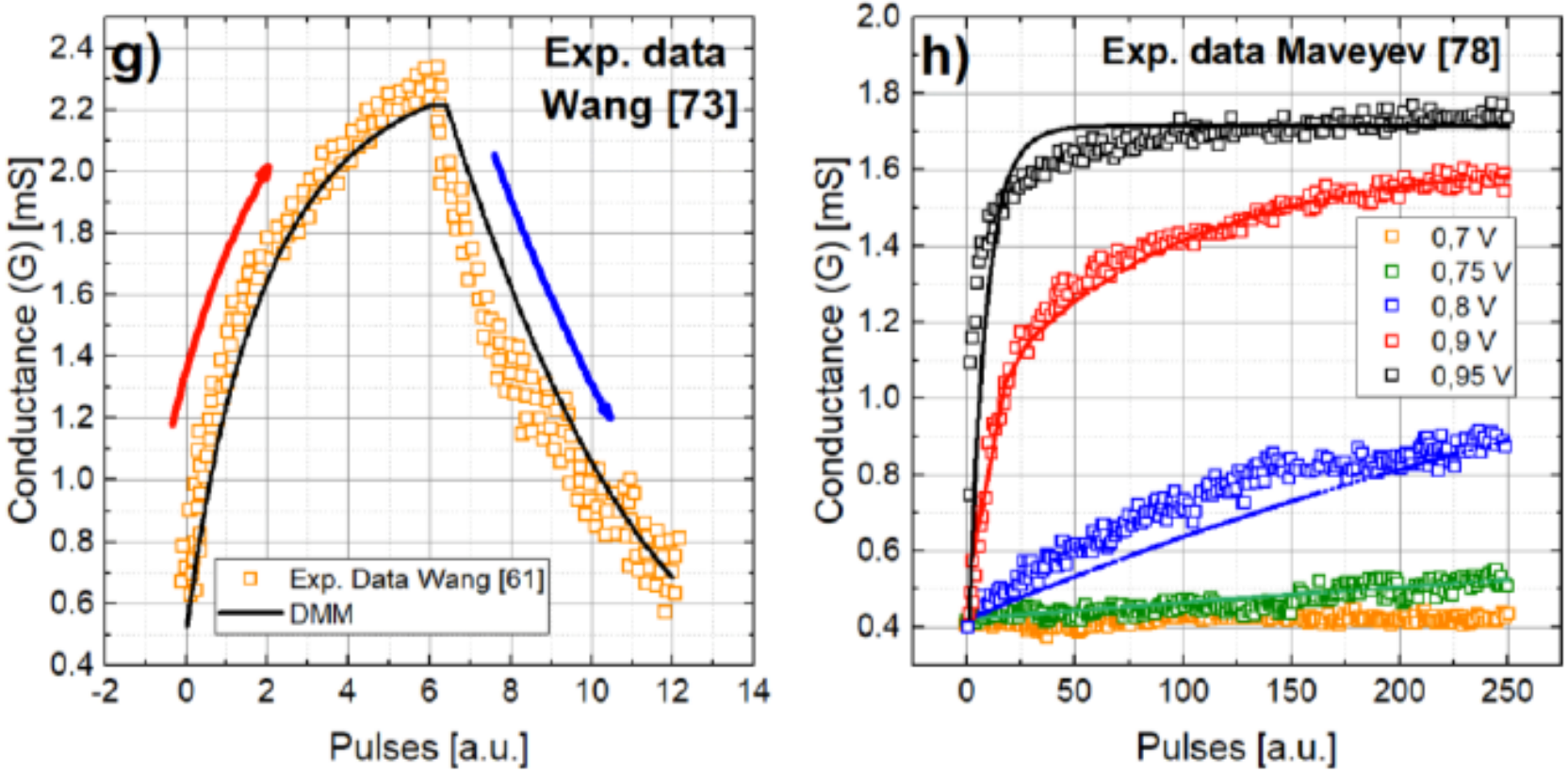
Differential equation represents a dynamic balance between SET and RESET

E. Miranda and J. Suñé, *IEEE Transactions on Nanotechnology*, 19, 837, (2020)

Fitting experiments



Synaptic behavior

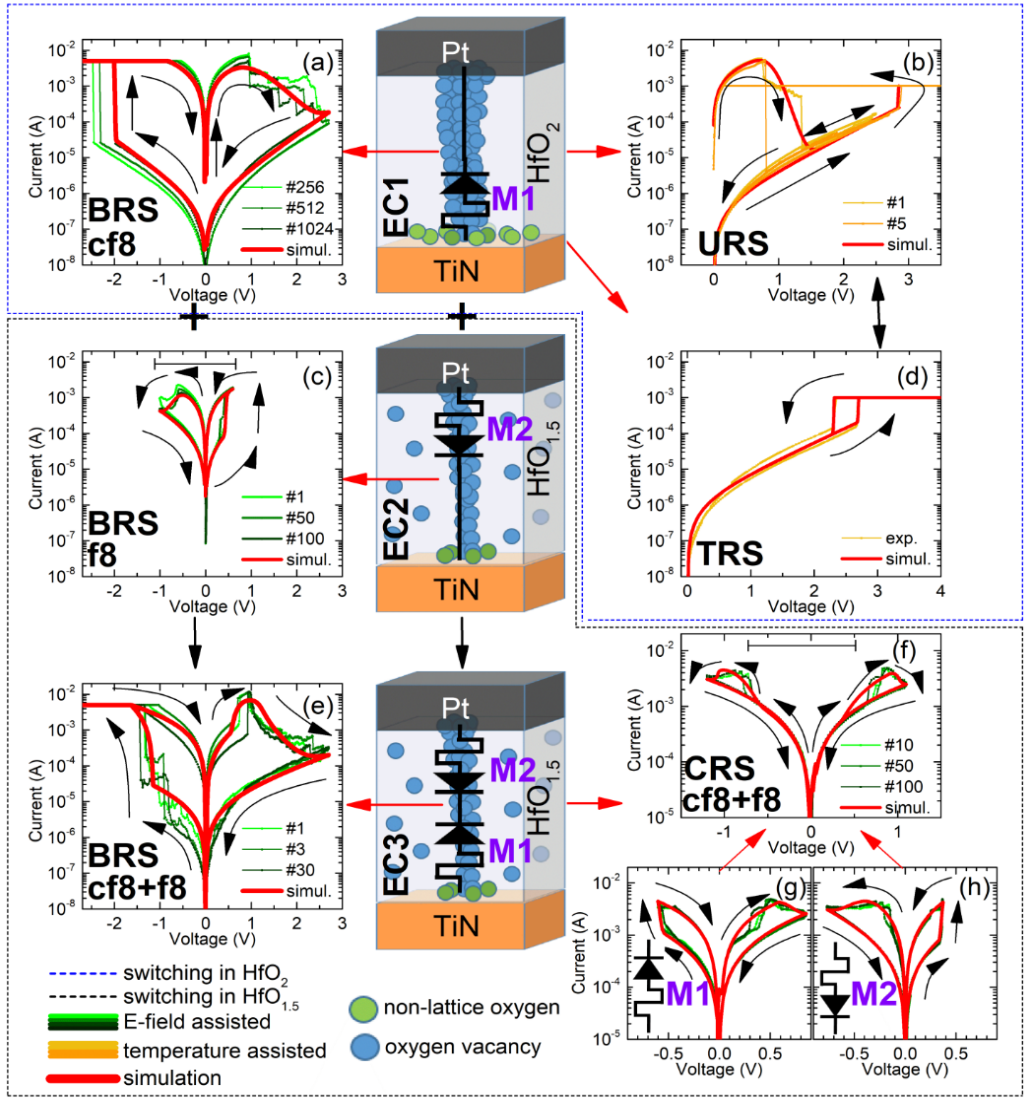


- Intermediate states are well-captured
- Potentiation/depression under the application of voltage pulses

Different switching modes

- Bipolar, unipolar, complementary and threshold switching

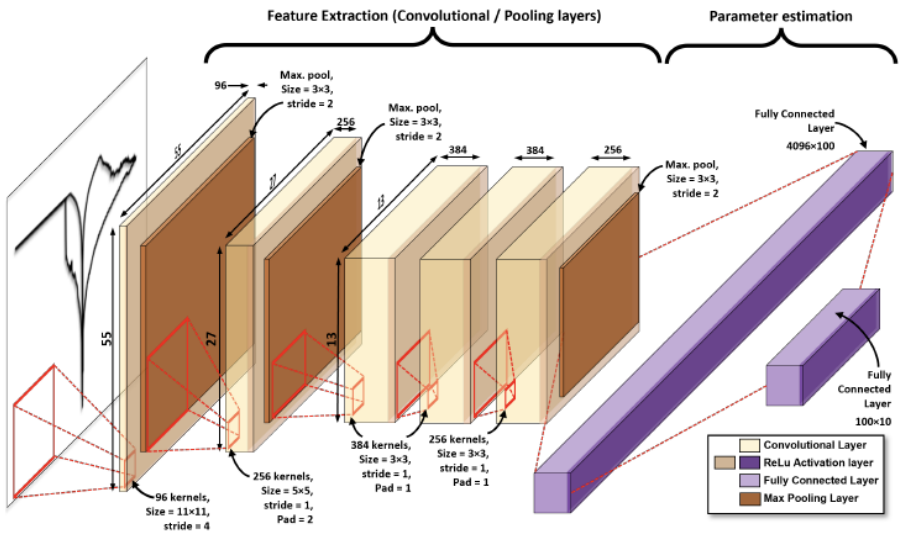
- Combining devices and/or changing switching rules.

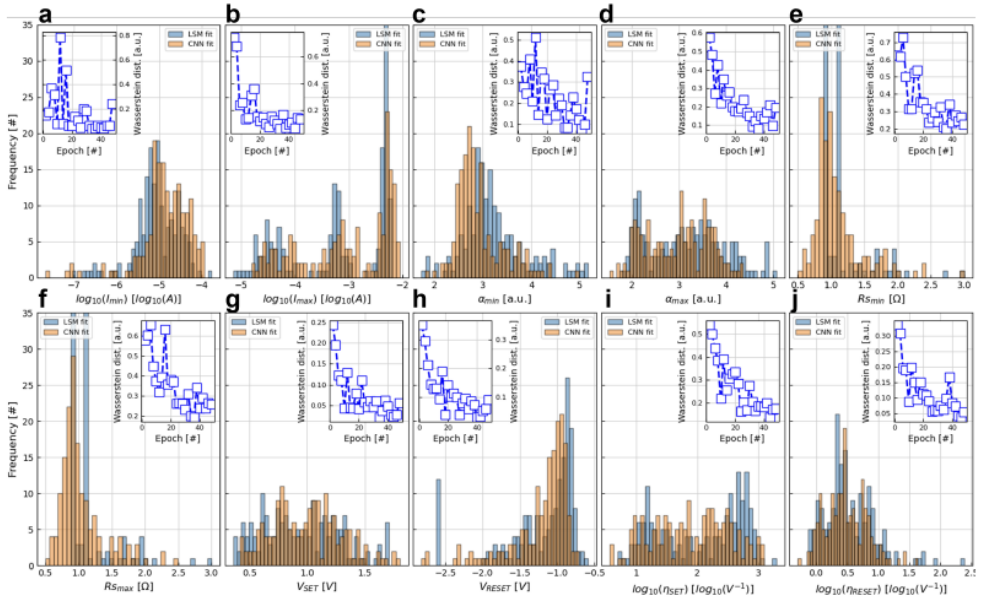


S. Petzold et al., *J. Appl. Phys*. **125**, 234503 (2019)

Extraction of parameters

Goal: Extraction of the 10 model parameters to fit experimental I(V) loops





- Convolutional neural network
- Supervised learning from (1000+200) graphical images of the I(V) loops.
- Labeling: iterative simulator-in the loop for systematic extraction of parameters.

F. Aguirre et al., Micromachines 13, 2002 (2022).

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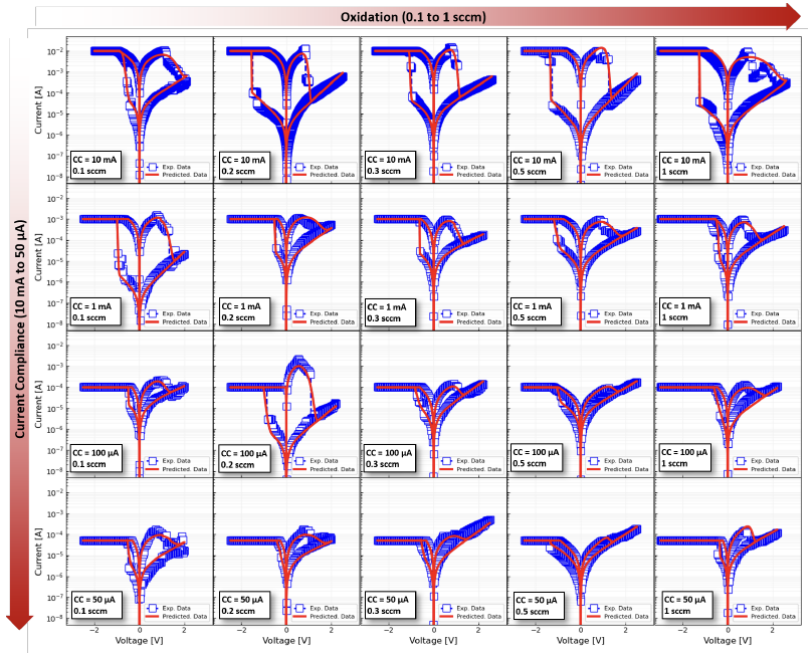
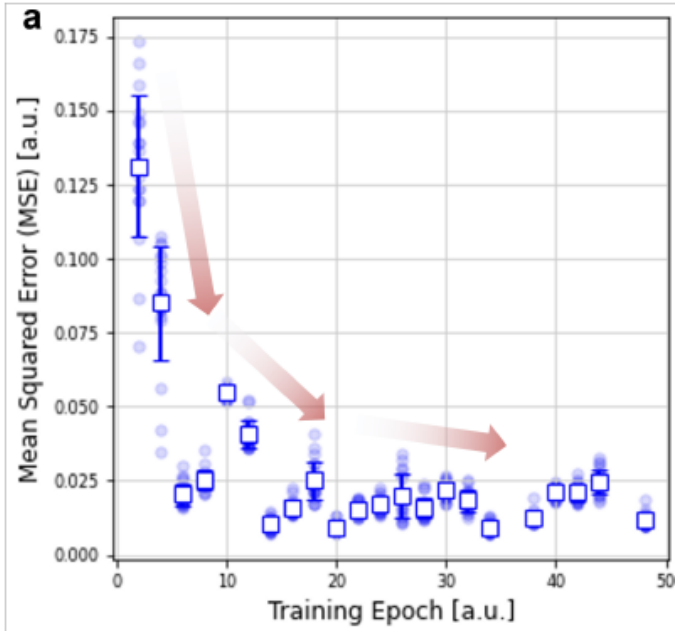
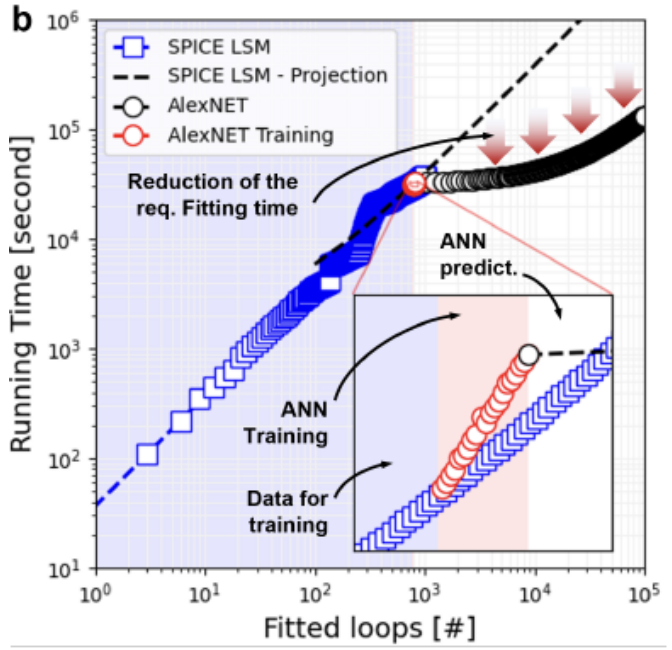




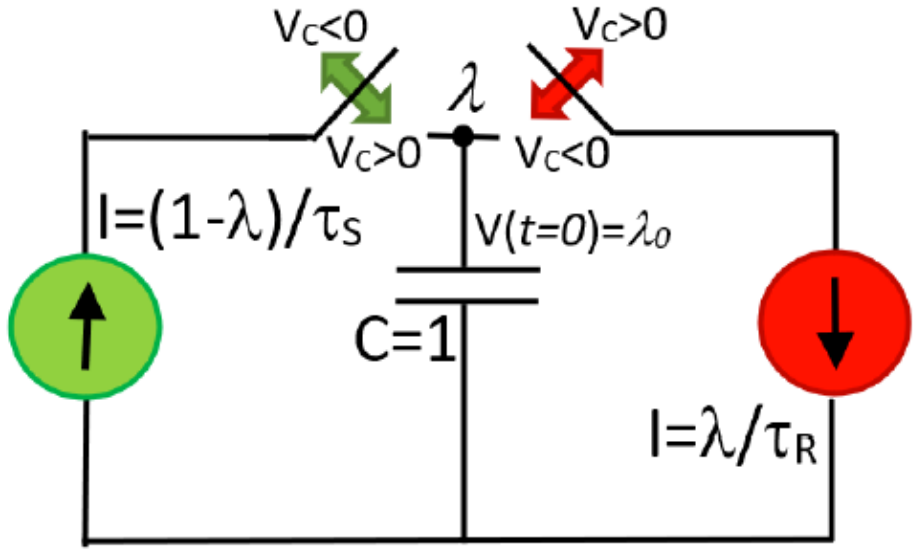


- Well-reproduced I(V) loops
- Less than 20 epochs are required for network training
- Significant advantage in extraction time for large number of loops (more than 10^3)

Equivalent circuit: SPICE

The state (memory) equation can be transformed into an equivalent circuit

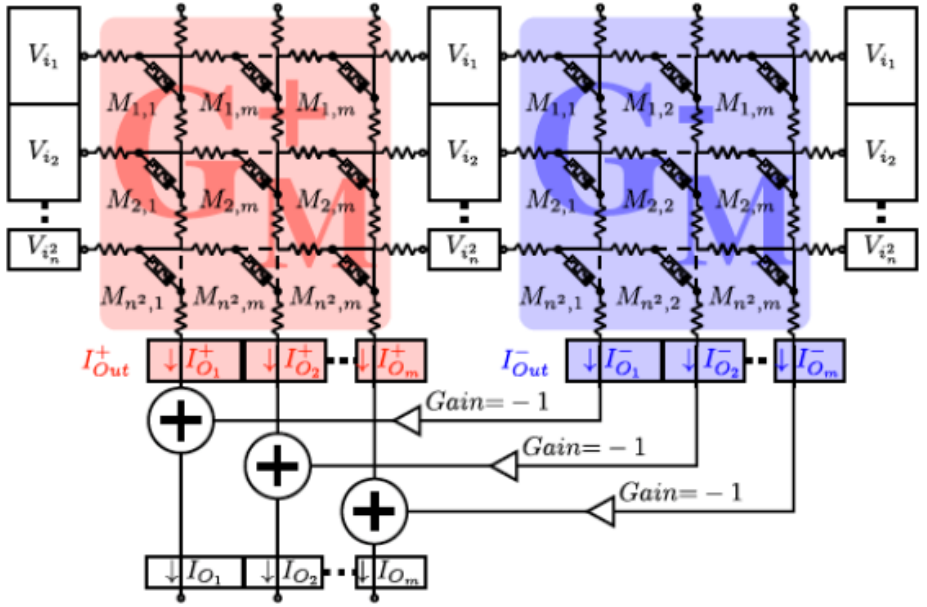
$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda,V_C)} - \frac{\lambda}{\tau_R(\lambda,V_C)}$$



- The SPICE motor is used to solve the differential equation
- SPICE simulation at the device and circuit levels

E. Miranda and J. Suñé, *IEEE Trans. on Nanotechnol.*, 19, 837, (2020)

Neural networks with SPICE



- Weights calculated in MATLAB and mapped into the memristors.
- 16K memristors and 20K MOSFETs (MNIST database)
- Writting the weights and inference phase.

F. Aguirre et al., IEEE Access, 8, 202174 (2020).

Neural network simulations

- In the **inference phase**, the state equation does not play any role (λ does not change) → QMM

- **Different figures of merit can be studied:** array size, line resistance, power consumption, network latency, variability, stuck@ faults,…

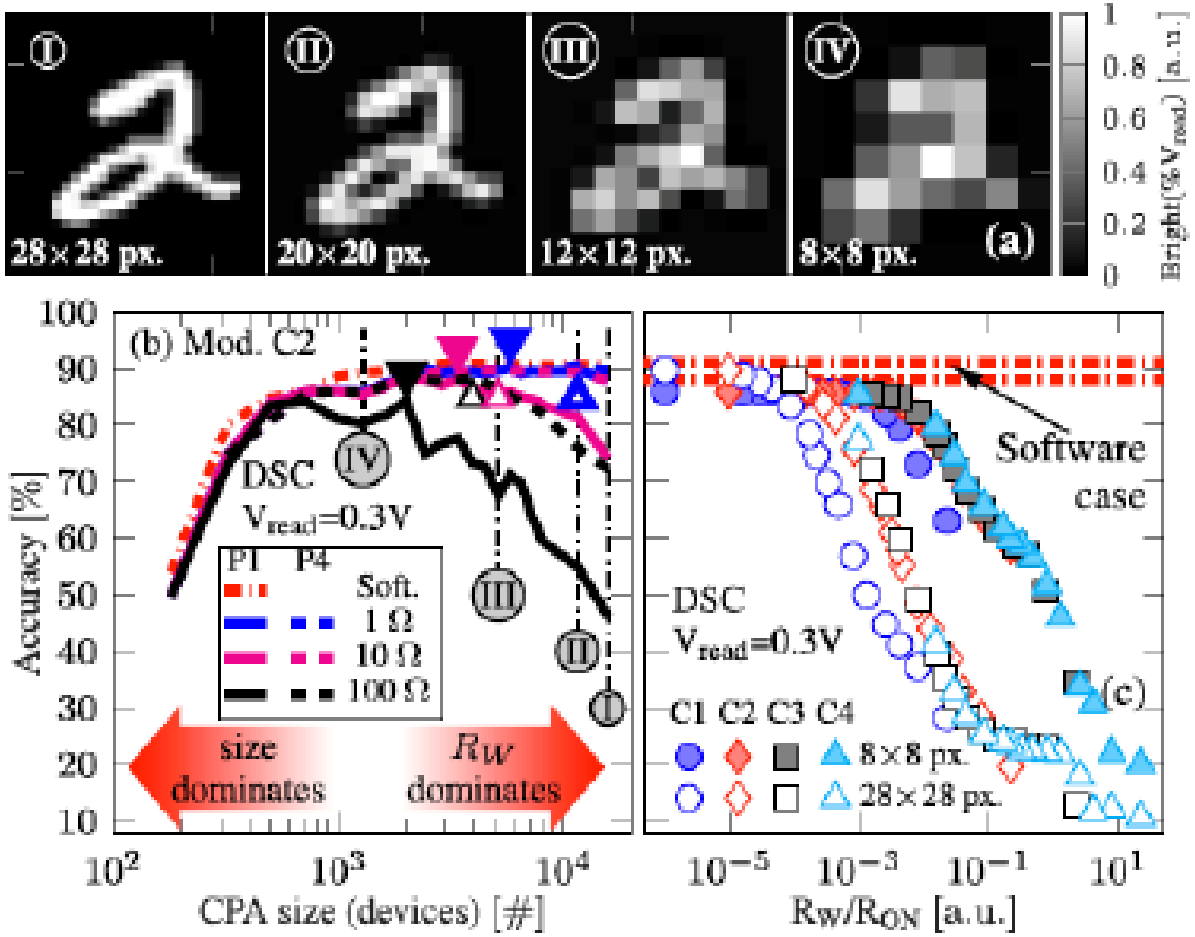
- **Training phase** : the coupling of internal state and current-voltage equations is required → DMM

Simulation of inference

One example:

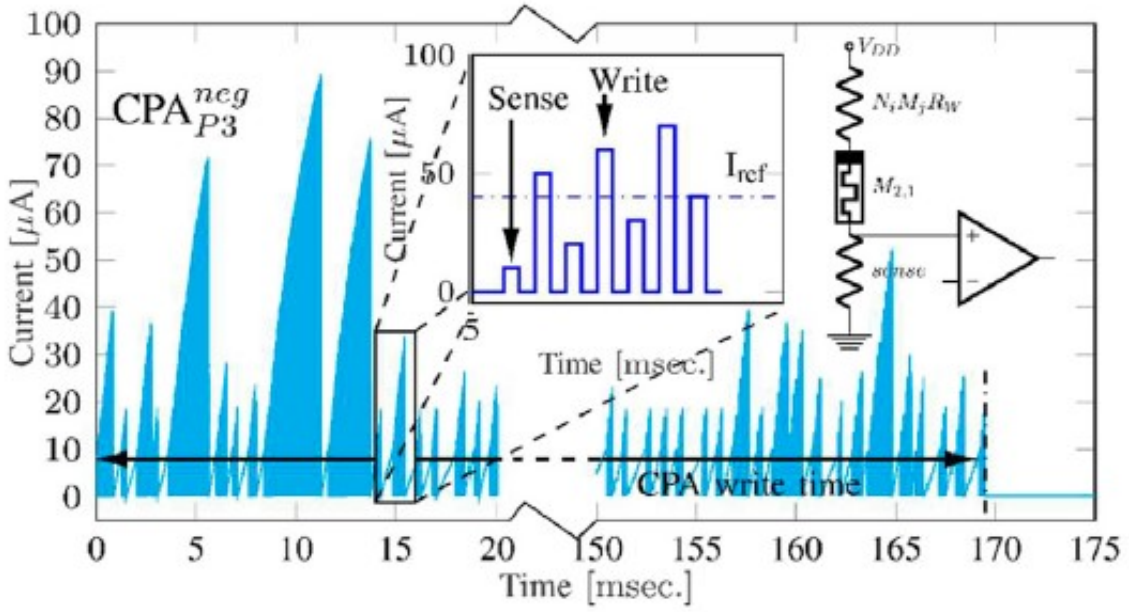
Impact of line resistance and CPA size

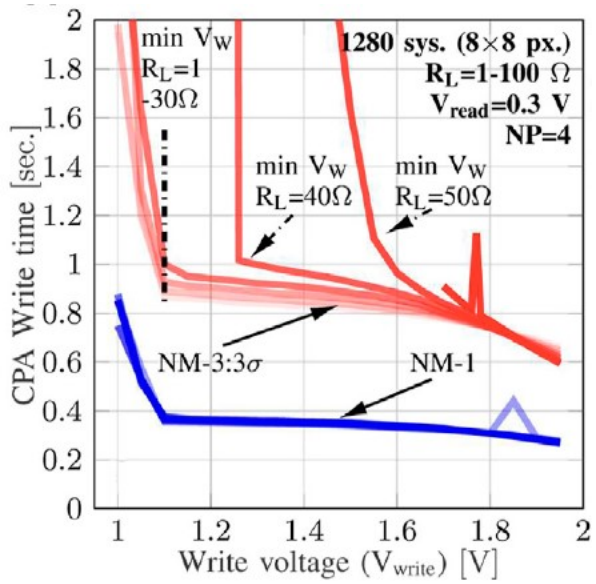
- Images resized from 28x28 px.
- For small CPAs, accuracy increases (small images are blurry)
- For large CPAs, accuracy degrades because of R_W effects.

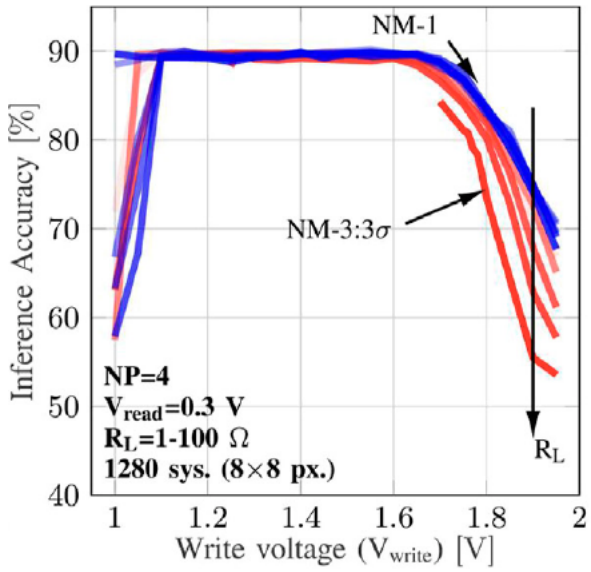


F. Aguirre et al., IEEE Access, 8, 202174 (2020).

Simulation of training (ex-situ)



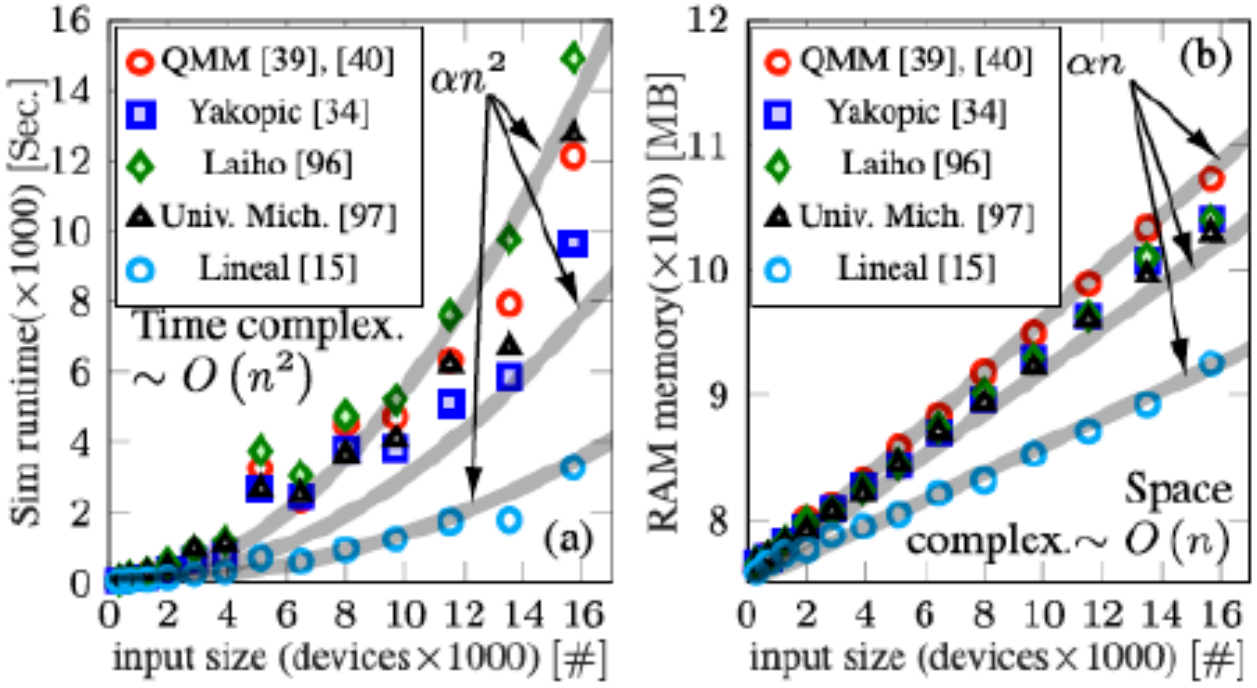




- Analyze different strategies for the mapping of weights onto the CPA
- Design the best programming protocols for inference accuracy
- Improve programming speed under realistic conditions (R_W)

F. Aguirre, J. Suñé and E. Miranda, Micromachines, 13, 303 (2022).

Model performace



- **Computational requirements:** simulation time and memory usage.
- Similar results but the DMM provides a **more accurate description**.

F. Aguirre et al., IEEE Access, 8, 202174 (2020).

Summary

- A compact behavioral model has been discussed
  - Differential internal-state memory equation
  - I(V) diode-like equation model inspired in the QPC
- The model can be implemented as an equivalent circuit for SPICE
- Different materials/device structures and different switching modes have been simulated
- A method for the extraction of parameters has been presented
- Simulation of neuromorphic circuits (16K).
- Computational resources comparable to other models with better accuracy

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Thank you very much!

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