Memristors with thousands of conductance levels for analog computing

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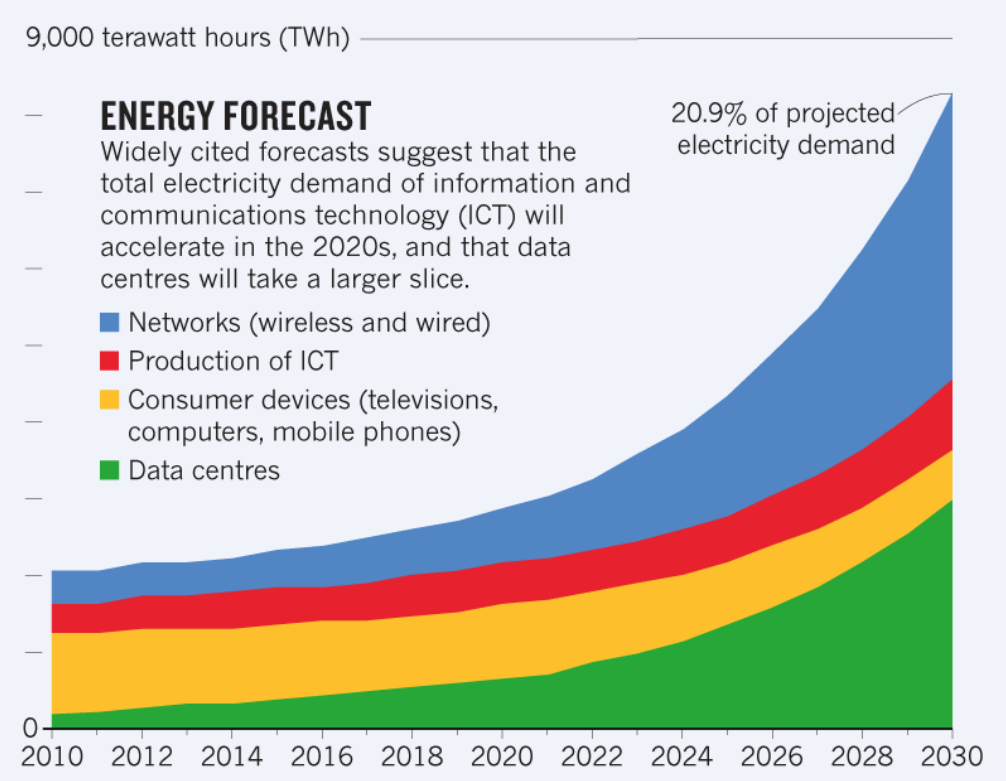
Unsustainable energy demand for computing



Solutions:

Rethink how to compute (**new paradigms**)
& where to compute (more **edge computing**)

Jones, Nicola. "How to stop data centres from gobbling up the world's electricity." *Nature* 561.7722 (2018): 163-167.

Andrae, Anders SG, and Tomas Edler. "On global electricity usage of communication technology: trends to 2030." *Challenges* 6.1 (2015): 117-157.

Analog data deluge at the edge

→ not feasible to be all converted and transmitted

→process in analog as much as possible

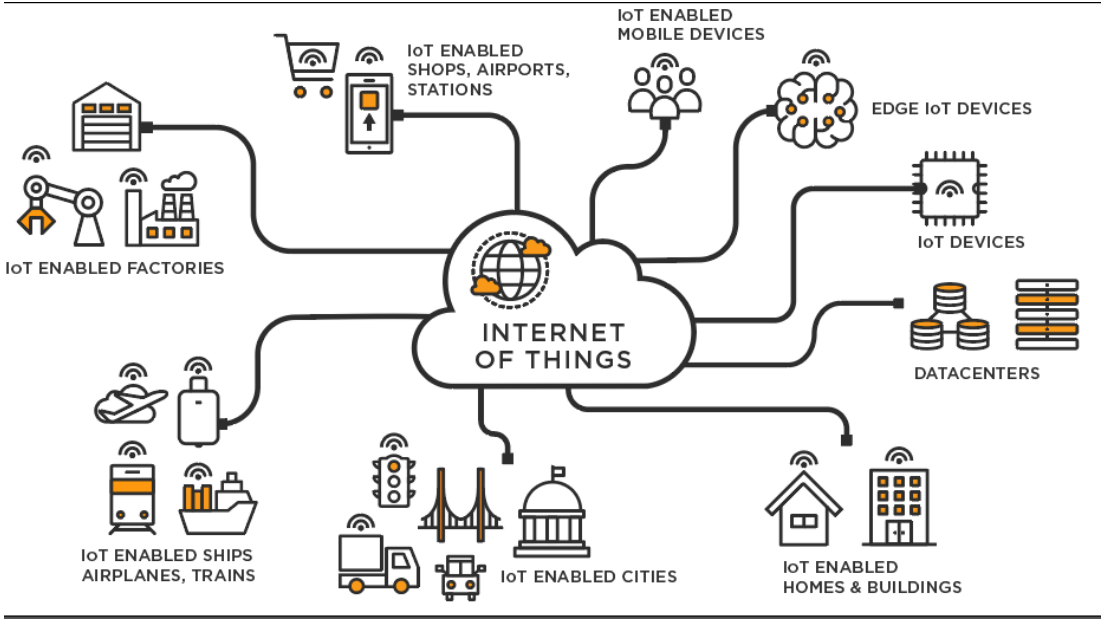
→process at the edge as much as possible

→analog circuits become increasingly more important

but

10% analog portion consumes 90% of total design time

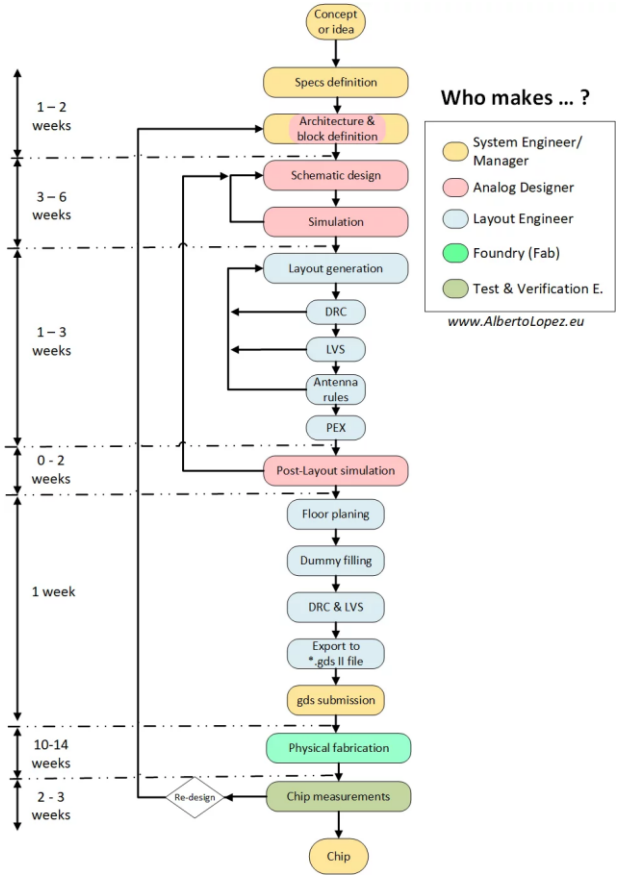
World is analog:
Physical signals are continuous in time and amplitude



FPAA is needed for analog circuits

0.5 year weeks for one iteration

2-3 iterations typically needed



How to quickly prototype digital circuits?

Field-Programmable Gate Arrays

(FPGAs)

How to quickly prototype Analog circuits?

Field-Programmable Analog Arrays

(FPAAs)

- Faster prototyping
- Design integration
- Improved component matching
- General purpose analog applications

Field-Programmable Analog Arrays (FPAAs)

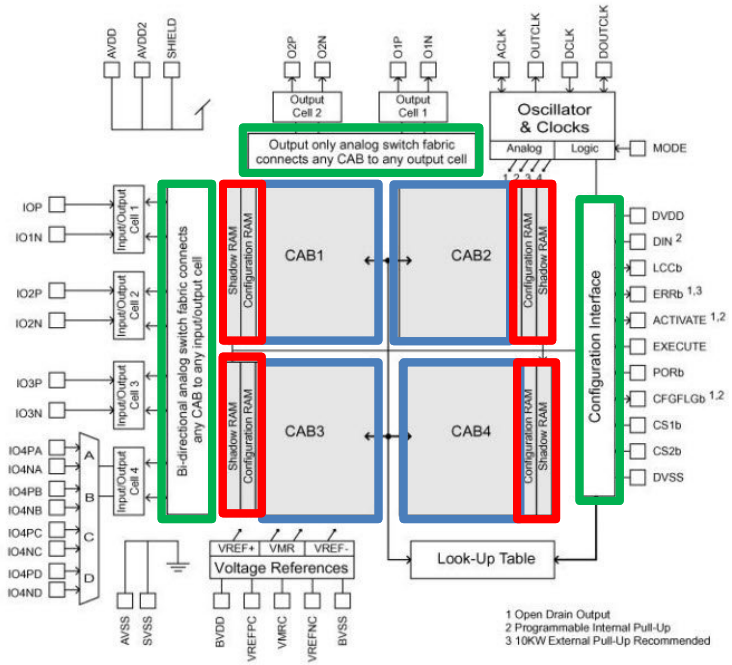
- **Configurable analog blocks (CABs)**
  - Amplification
  - Integration
  - Differentiation
  - Addition
  - Subtraction
  - Multiplication
  - Comparison
  - Log, exponential…

A major challenge: Lack of appropriate analog components!

How about memristors?

- **Reconfigurable routing network (switching matrix)**
- **memory elements used to define both the function and structure (configuration memory)**

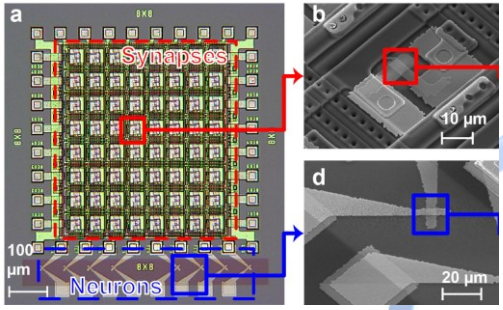
Early FPAA designs



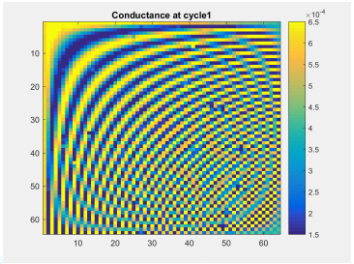
The architecture of AN221E04 FPAA dpASP chip.

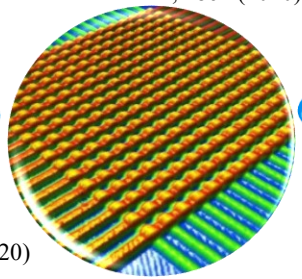
Our studies of memristors for computing

Natural Intelligence



Improved speed-energy efficiency





Artificial Synapses

Nature Comm. **8**, 752 (2017)
Nature Materials **16**, 101 (2017)
Science **364**, 570 (2019)
Sci. Adv. **6**, eaba6173 (2020)
Nature Comm. **11**, 1861 (2020)

Artificial Neurons

Nature Electronics **1**, 137 (2018)
Nature Comm. **9**, 3208 (2018)
Nature Comm. **11**, 51 (2020)
Nature Nanotechnology **15**, 776 (2020)

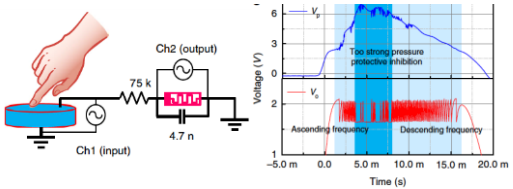
ML Accelerators

Nature Electronics **1**, 52 (2018)
Nature Comm. **9,** 2385 (2018)
Adv. Mater. **29**, 1705914 (2018)
Nature Machine Intelligence **1,** 49 (2019)
Nature Electronics **2**, 115 (2019).
Nature Machine Intelligence **1,** 434 (2019)
Nature Electronics **3**, 409 (2020)
Nature **577**, 641 (2020)
Sci. Adv. **7**, eabj4801 (2021)
Nature **615,** 823 (2023)

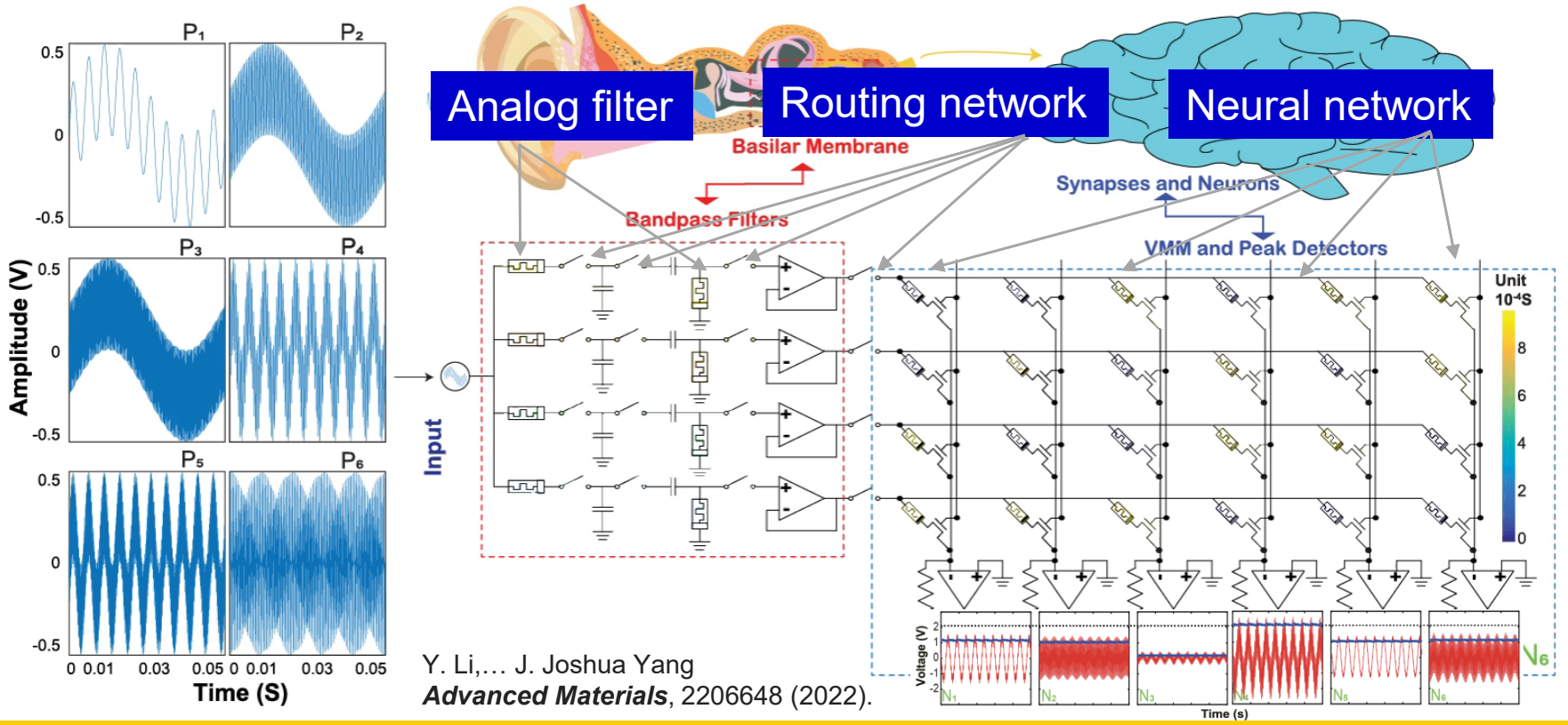
Intelligent Systems

Nature Comm. **8**, 882 (2017).
Nature Comm. **8**, 15666 (2017).
Adv. Mater. **29**, 1604457 (2017).
Adv. Mater. **31**, 1902761 (2019)
Nature Materials **18**, 309 (2019).
Nature Electronics **3**, 225 (2020)
Nature Materials **16**, 396 (2017).
Nature Comm. **9**, 417 (2018)
Nature Electronics **1**, 130 (2018).
Nature Electronics **1**, 548 (2018).
Nature Nanotechnology **14**, 35 (2019).
Nature Review Materials **5,** 173 (2020)

Sensing System For Robotics



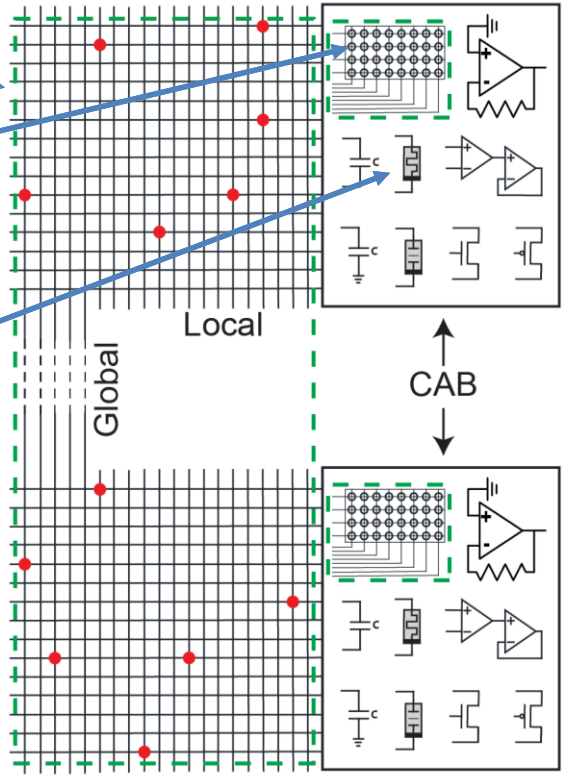
Memristor FPAA
(Mixed-frequency Signal Classifier - experiments)



Y. Li,… J. Joshua Yang
Advanced Materials, 2206648 (2022).

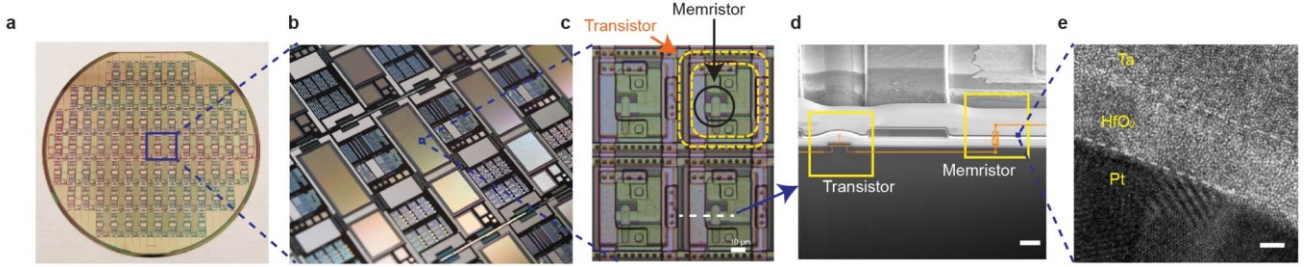
What do we need for large-scale FPAA?

1. Large cross-bar arrays
2. Low current and analog memristors
3. Many conductance levels

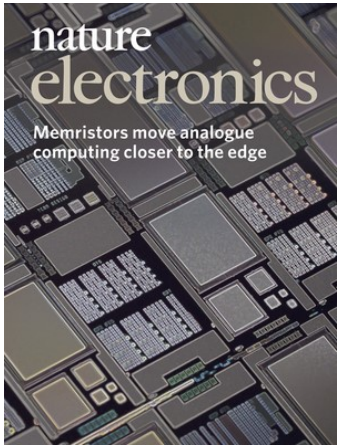


Y. Li,… J. Joshua Yang, “Memristive Field-Programmable Analog Arrays for Analog Computing.” ***Advanced Materials***, 2206648 (2022).

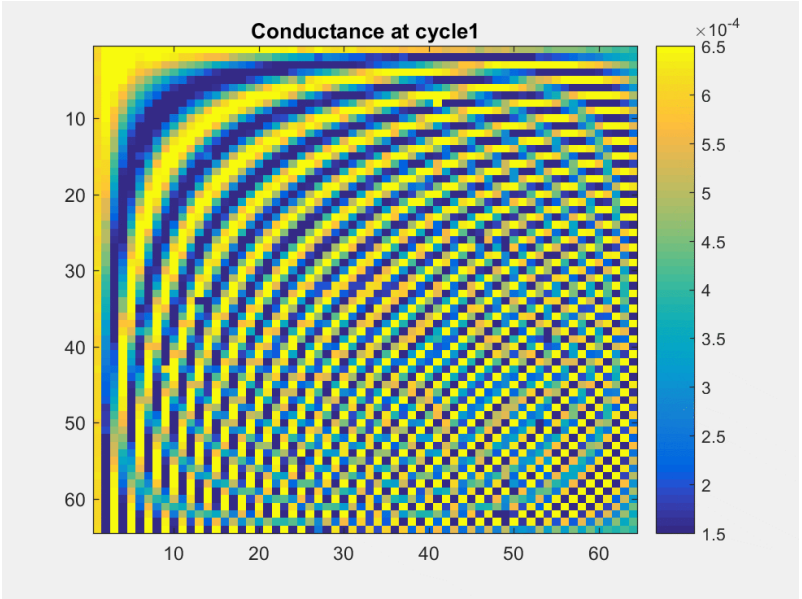
1. Large cross-bar arrays (previous demos, 128 x 64)



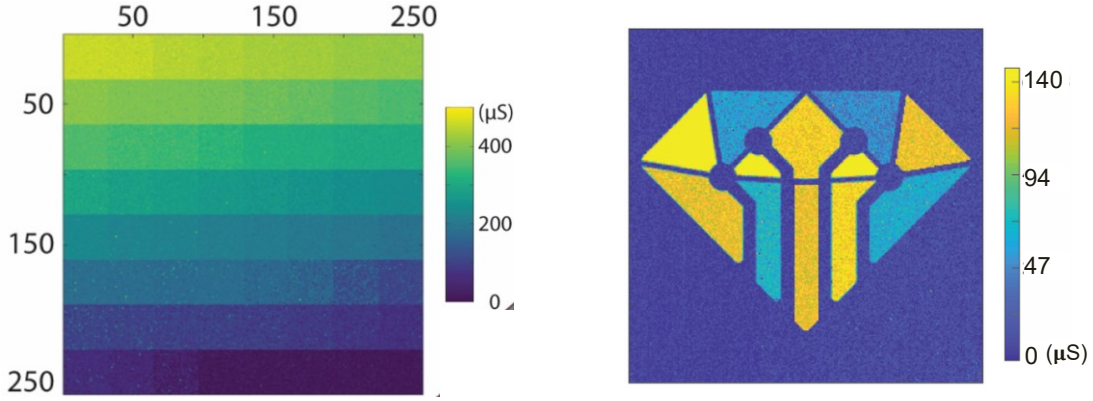
Li et al., Nature Electronics **1**, 52 (2018).

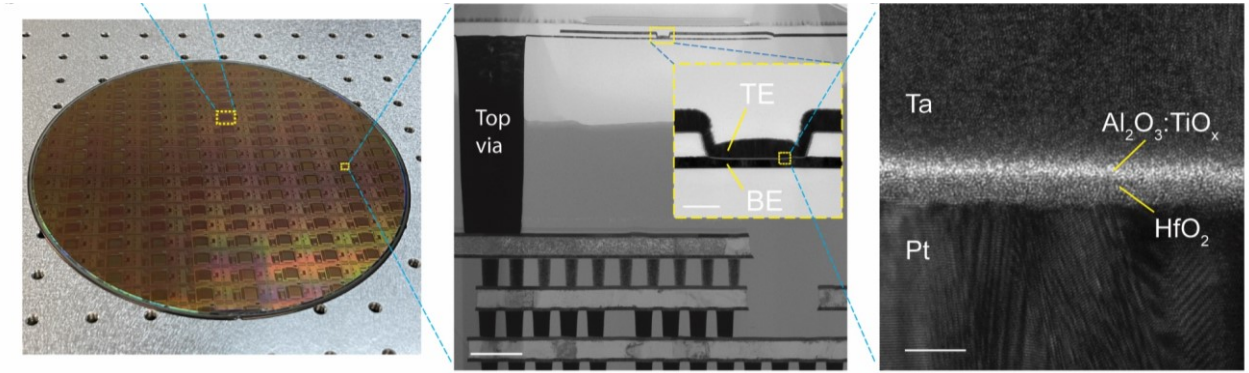


(Cover image of inaugural issue)



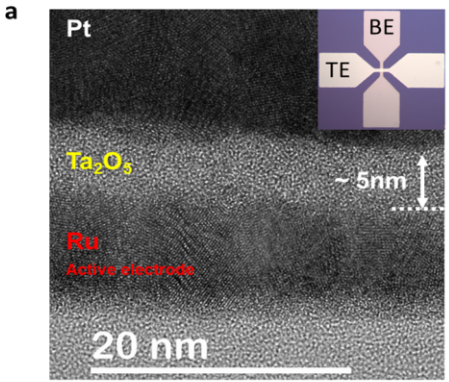
Latest arrays: 256 x 256 integrated on CMOS

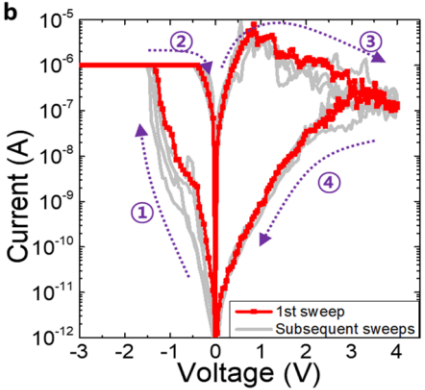


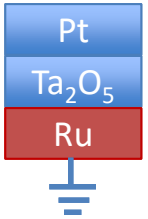


M. Rao,…,J. Joshua Yang "Thousands of conductance levels in memristors integrated on CMOS", **Nature** 615, 823-829 (2023).

2. Low current and analog devices

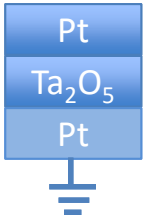


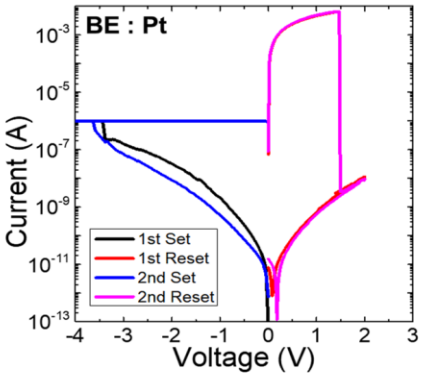


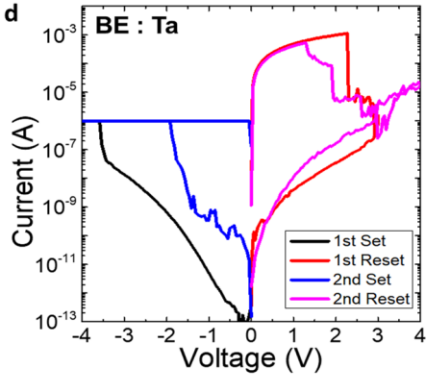


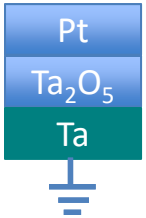
For neural network:
Low currents
Gradual switching

5 x 5 um^2







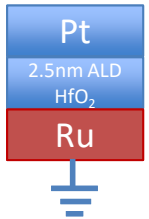


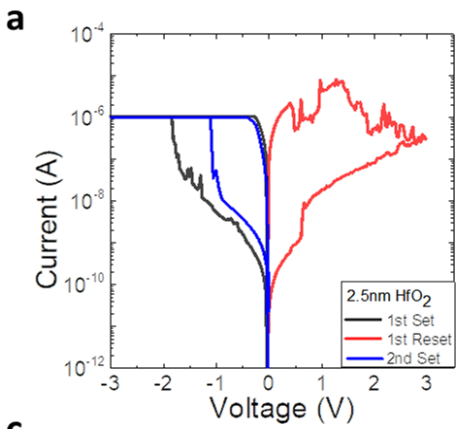
For routing network:
Abrupt switching
Large ON/OFF ratio

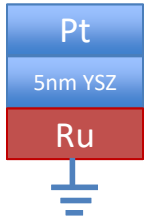
J. Yoon,…, J. Joshua Yang, Adv. Mater. **32**, 1904599 (2020)

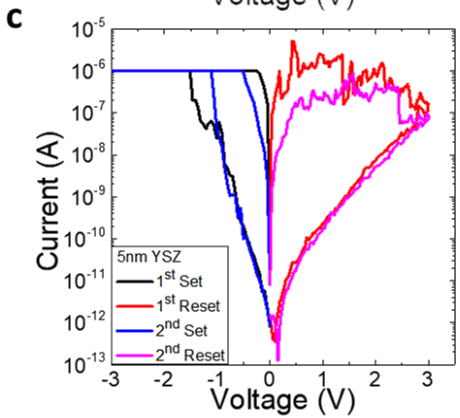
Oxide type insensitive

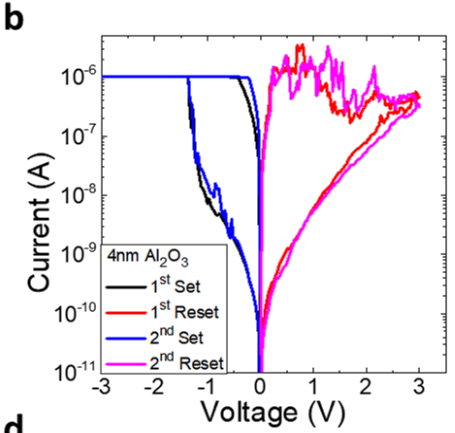
Signatures:
Low currents
Gradual reset

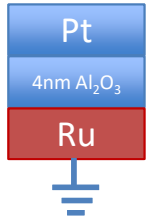


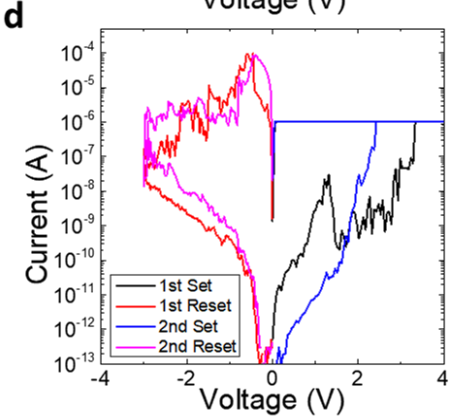


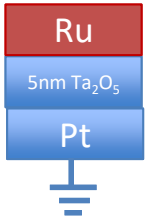








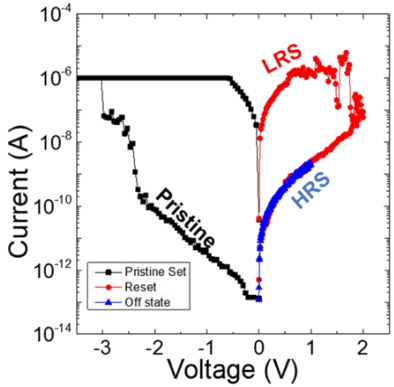


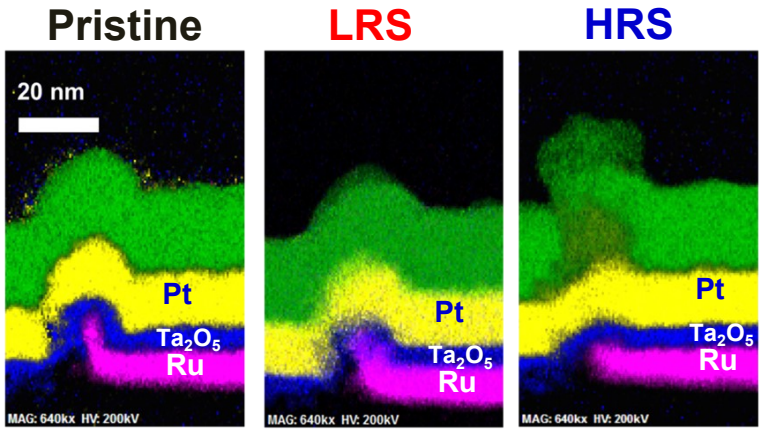


J. Yoon,…, J. Joshua Yang, Adv. Mater. **32**, 1904599 (2020)

Evidence of Ru conduction channel: ex-situ TEM

Collaborator: Yuzi Liu, ANL





J. Yoon,…, J. Joshua Yang, Adv. Mater. **32**, 1904599 (2020)

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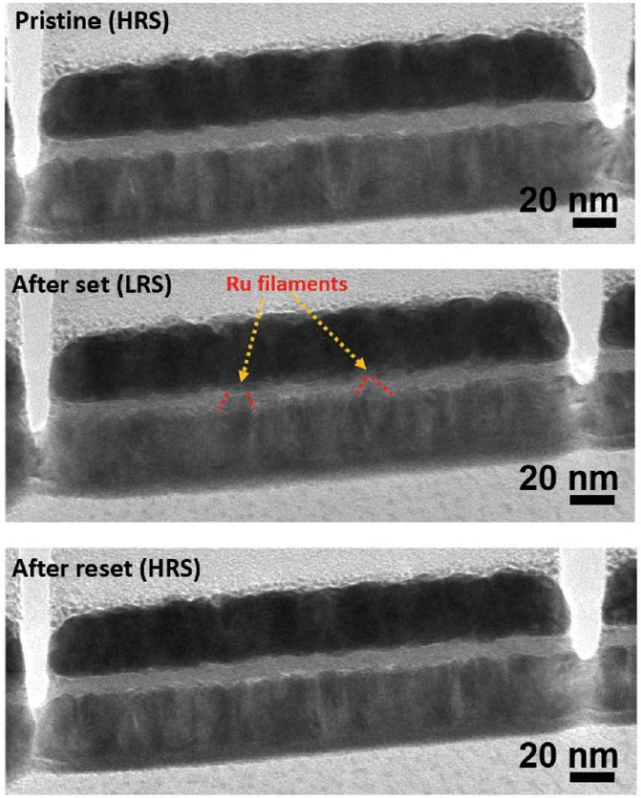
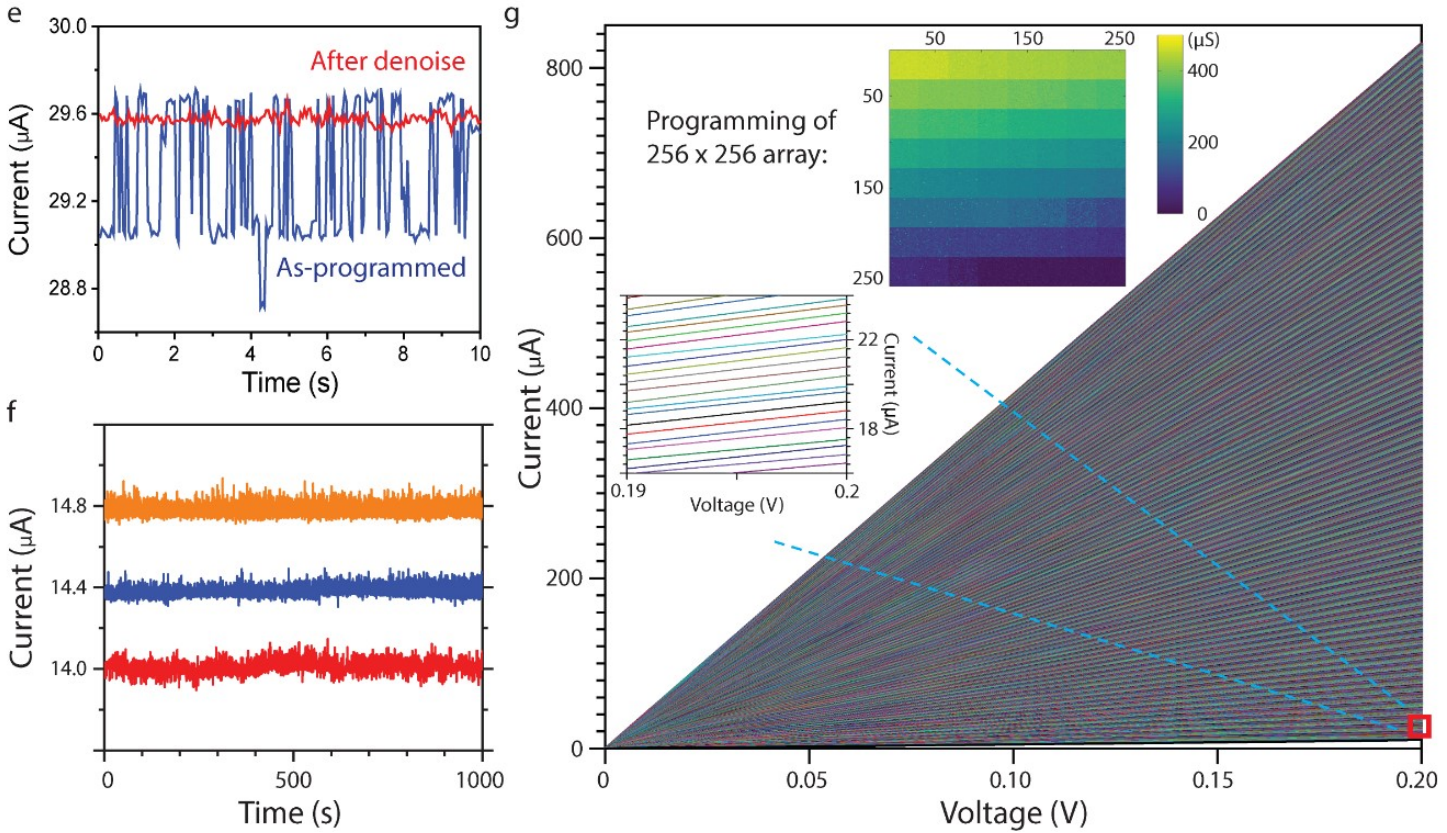


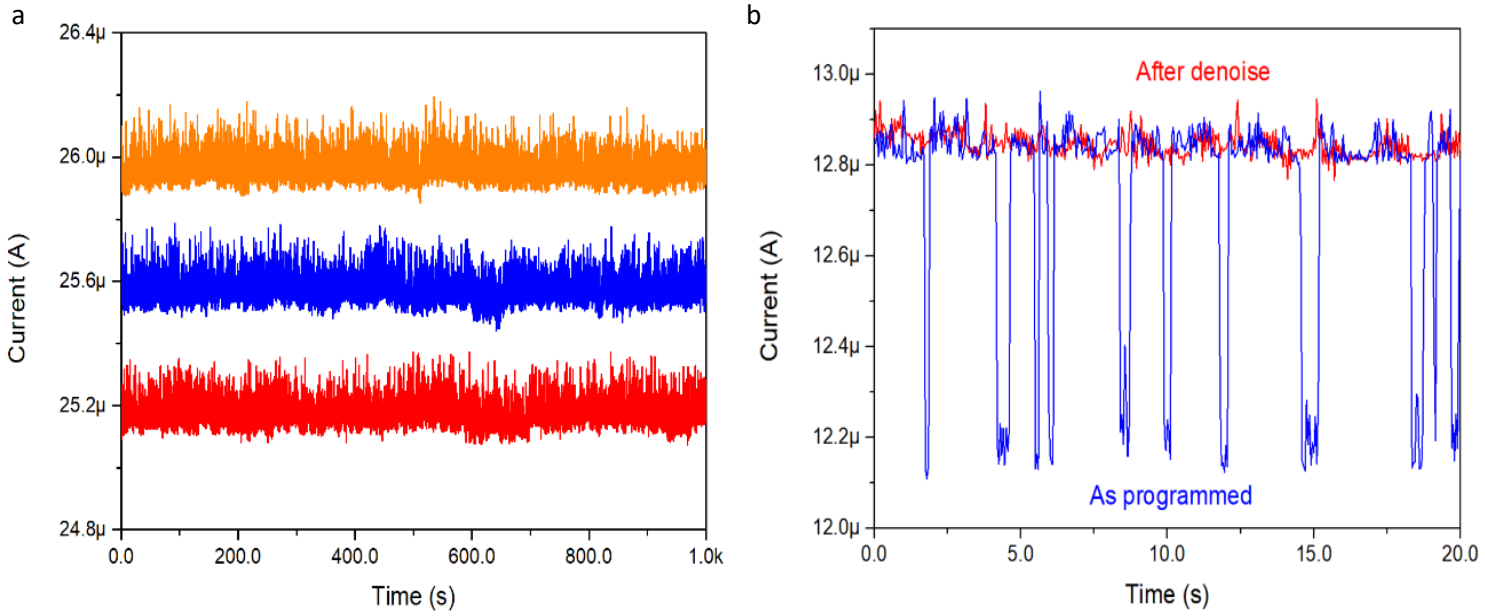
J. Yoon,…, J. Joshua Yang, Adv. Mater. **32**, 1904599 (2020)

3. 2048 resistance levels in one device



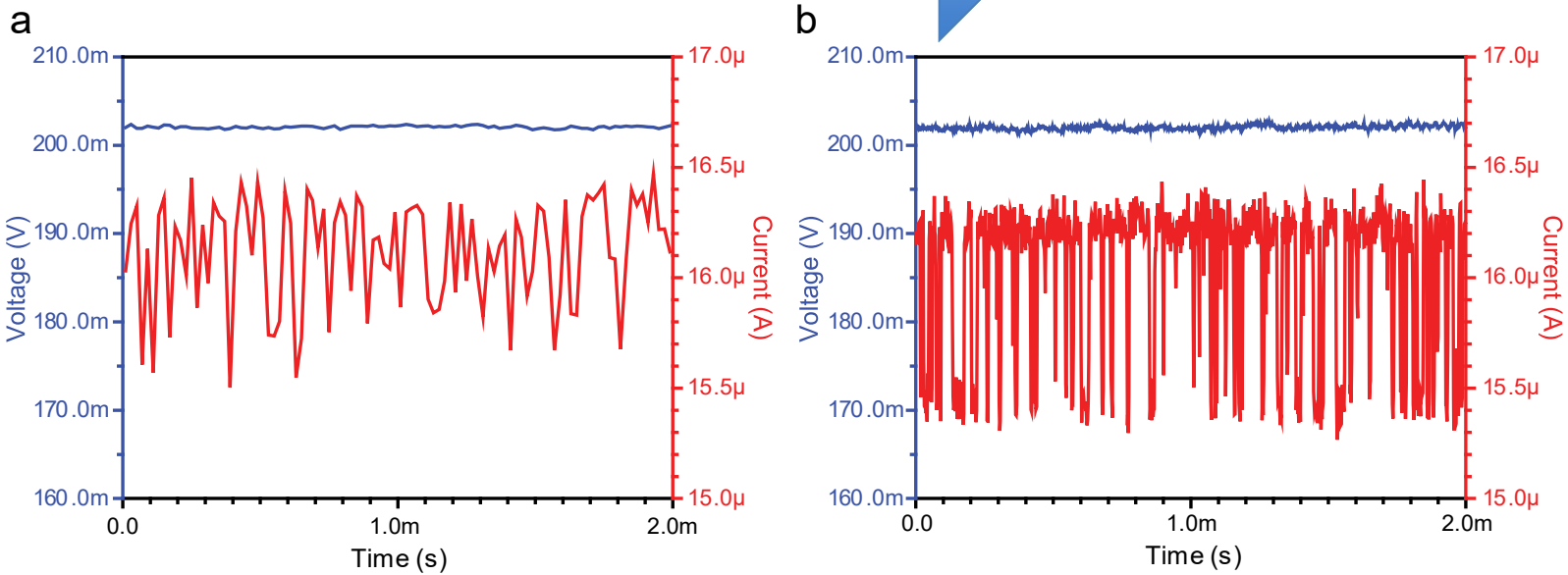
M. Rao et al., J. Joshua Yang "Thousands of conductance levels in memristors integrated on CMOS", **Nature** 615, 823-829 (2023)

Other oxides: TaOx



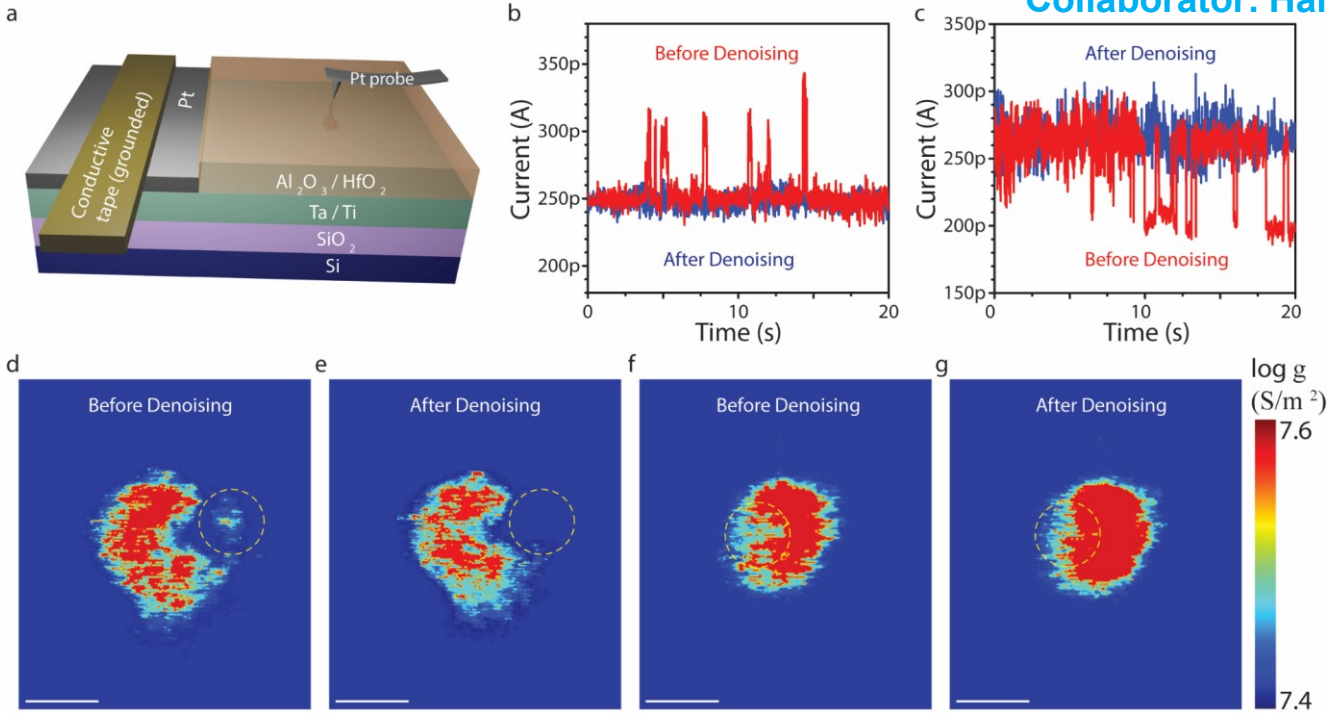
RTN or not?

RTN or not? → High sampling rate → Confirmed RTN



Mechanisms: experimental observations

Collaborator: Han Wang, USC



Island **"Incomplete Channel" doped with less Vos ➔RTN** **bay**

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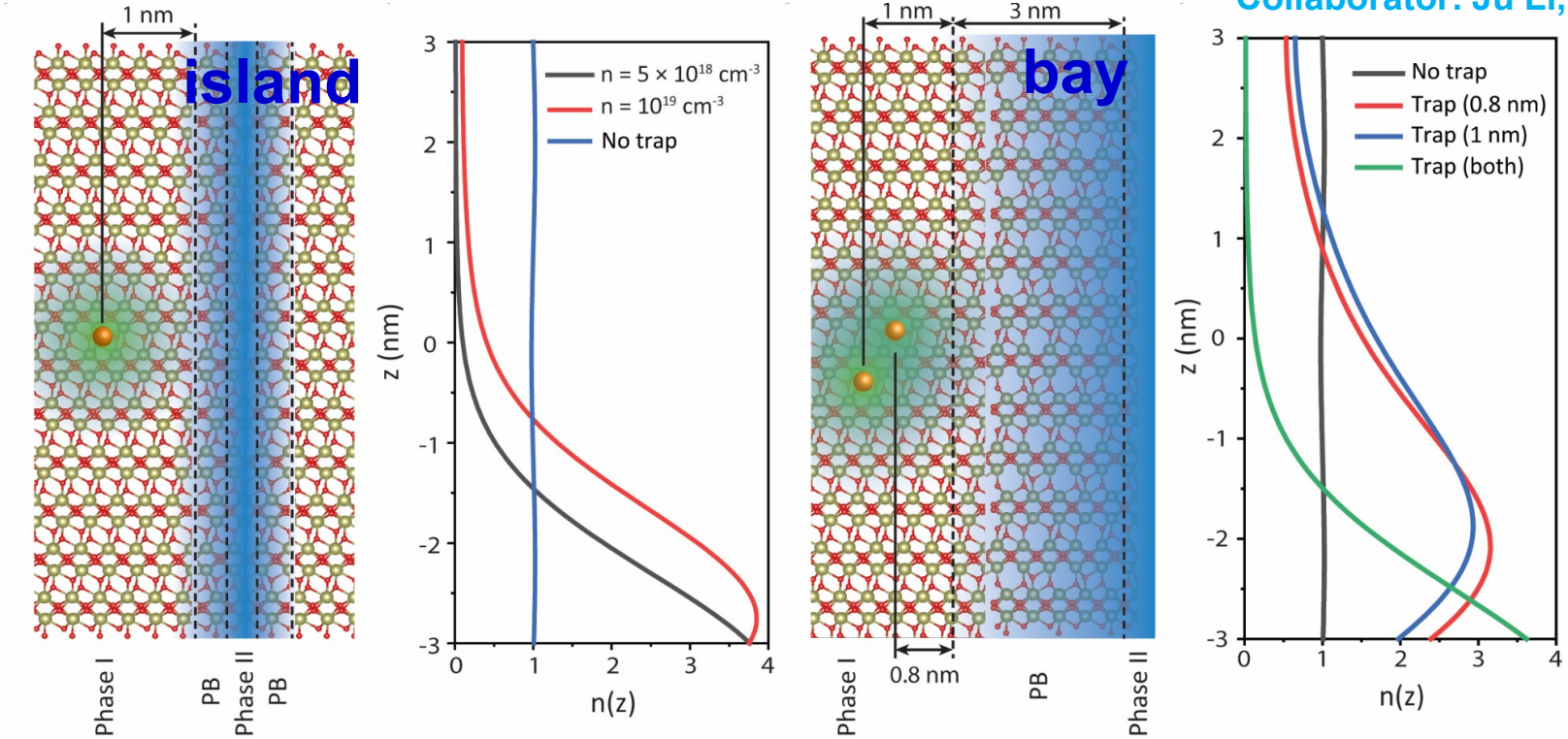
Mechanism: theoretical rationalization

Collaborator: Ju Li, MIT



Lightly doped with Vo

➔More sensitive to trap-blocking

denoising

Eliminate the sensitive parts – "lightly doped regions"

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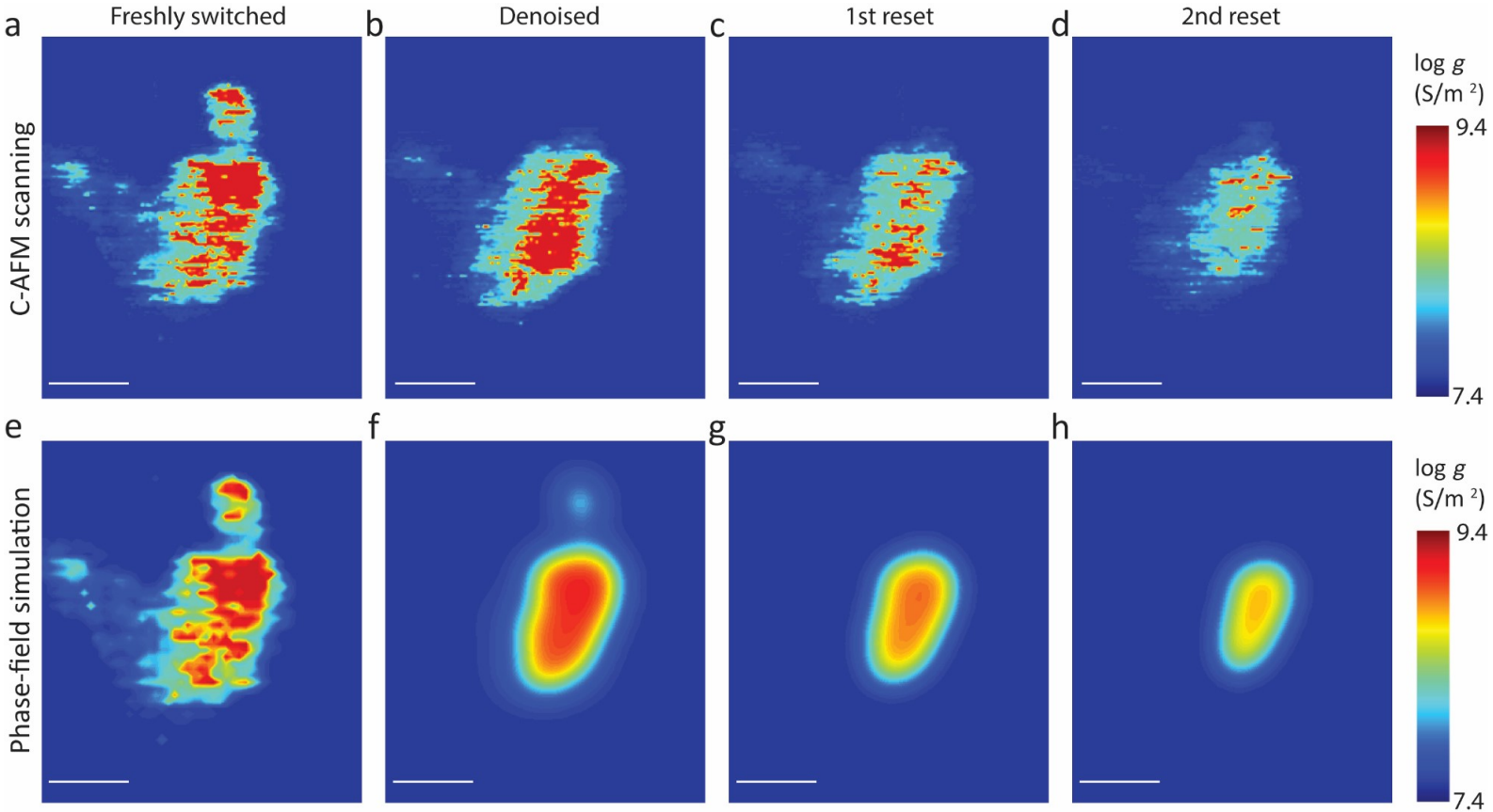
Mechanism of denoising

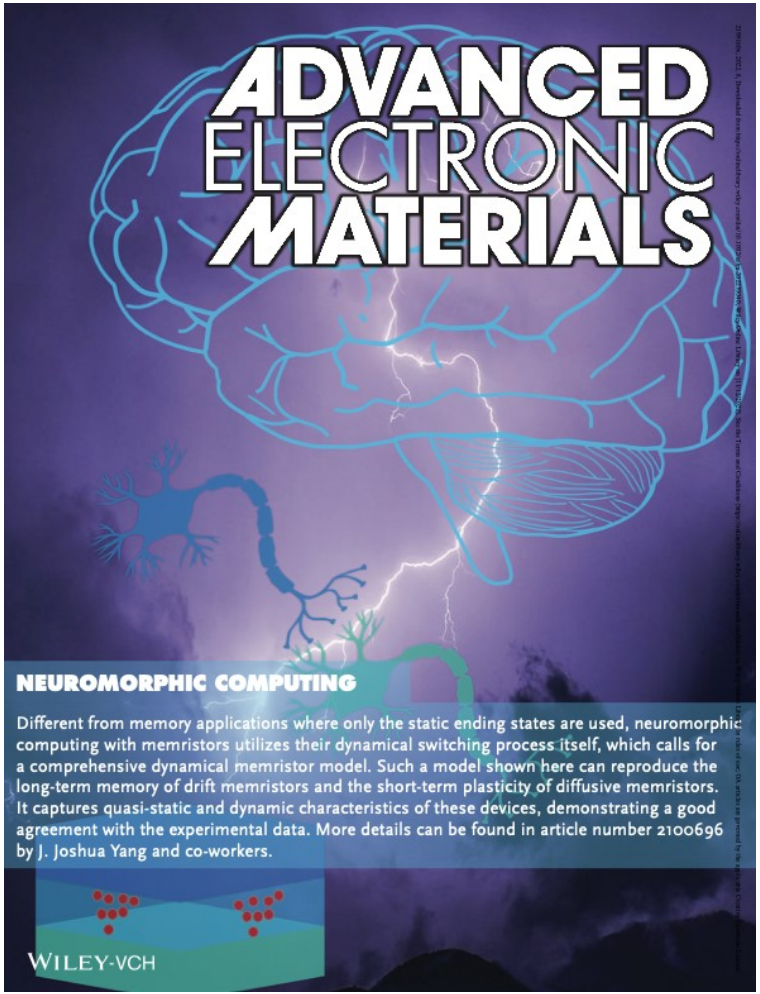


M. Rao et al., J. Joshua Yang "Thousands of conductance levels in memristors integrated on CMOS", **Nature** 615, 823-829 (2023)

A Dynamical Compact Model of Diffusive and Drift Memristors for Neuromorphic Computing

Ye Zhuo, Rivu Midya, Wenhao Song, Zhongrui Wang, Shiva Asapu, Mingyi Rao, Peng Lin, Hao Jiang, Qiangfei Xia, R Stanley Williams, J Joshua Yang

Advanced Electronic Materials 8, 2100696 (2022)



Summary:

- FPAAs may provide a great boost to analog circuits, which are increasingly more important.
- memFPAA has been demonstrated with memristors playing three critical roles: routing network (binary), analog components (analog) and neural networks (low-current and gradual).
- Revealed the origin of RTN noise, devised a protocol to eliminate it and obtained thousands of conductance levels.
- Demonstrated chips with 256x256 arrays fully integrated on CMOS circuitry.

Acknowledgements:

Postdoc and students: Mingyi Rao, Wenhao Song, Ye Zhuo, Zhongrui Wang, Saumil Joshi, Jungho Yoon, Rivu Midya,, Navnidhi Upadhyay

- Collaborators:
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- R. Stan Williams, TAMU
- John Paul Strachan, Hewlett Packard Labs
- Sergey E. Savel'ev, Loughborough University
- Hai (Helen) Li, Duke University
- Alec Talin, SNL
- Alberto Salleo, Stanford University
- Qinru Qiu, Syracuse University
- Han Wang, USC
- Ju Li, MIT
- Miao Hu, Ge Ning, TetraMem

Acknowledgements:

AFRL (RI & RX)

DARPA

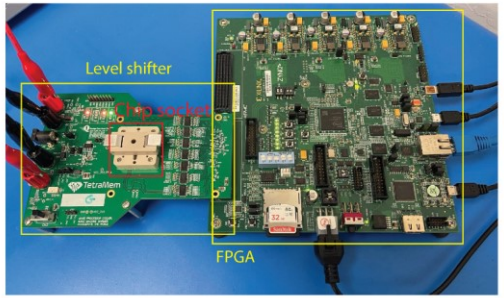
NSF

AFOSR (MURI)

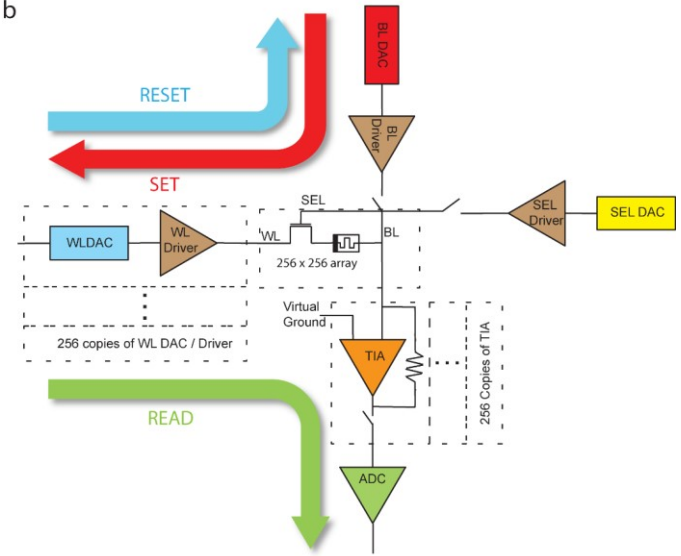
IARPA

Testing setup

a



b



Denoising cost