Efficient Method to Obtain Target Bias Solutions of 6F² DRAM Cells with Geometric Fluctuations

Geonho Park, Seung-Cheol Han, and Sung-Min Hong

School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology E-mail: <u>smhong@gist.ac.kr</u>

ABSTRACT

A machine learning (ML)-TCAD algorithm is implemented to obtain the target bias solution of dynamic random access memory (DRAM) cells efficiently, which are generated by introducing geometric fluctuations into the ideal cell structure. The light gradient boosting machine (LGBM) trained on the electrostatic potential profiles of DRAM cells is used to predict the initial solutions at specific bias conditions. The model is trained with 300 simulation results. Using the proposed method, solutions for 1,000 devices at a target bias are obtained quickly.

INTRODUCTION

Geometric fluctuations during DRAM manufacturing obviously affect transistor performance and yield [1]. Therefore, a simulation considering these variations is important, but it requires a lot of computational time. Since the device characteristics are sensitive to geometric fluctuations, a perturbative approach is difficult to apply and we must perform the full device simulation for each device. To overcome this drawback, the ML-TCAD framework has been widely used in this field recently [2]. However, sophisticated and high-level ML/AI models such as CNN and U-net are required.

In this work, we propose an efficient simulation flow using an easy-to-use Light Gradient Boosting Machine (LGBM) [3] to obtain the target bias solutions of DRAM cells with geometric fluctuations.

LGBM MODEL AND RESULTS

We built an LGBM model to predict the electrostatic potential profile of $6F^2$ DRAM in **Fig. 1**. As shown in **Fig. 2**, device parameters (L_{G1,2}, L_{ov}, T_{ox}, H_{fin}, R_{iso}, N_{sd}, and N_{ch}) and spatial parameters (x, y, z coordinates) are used as input parameters to the model. The electrostatic potential profile at a given position is obtained as an output. For high accuracy of the model, spatial parameters are preprocessed using the K-means clustering.

The entire simulation procedure to obtain the target bias solution of DRAM cells is shown in **Fig. 3**. First, an LGBM model is trained using the electrostatic potential profiles of 300 DRAM cells, which are generated by introducing geometric fluctuations into the ideal cell structure. These profiles are obtained with our in-house simulator, G-Device [2]. The drift-diffusion model is solved with the doping-dependent mobility model (Masetti), the inversion layer mobility model (Lombardi), the high-field saturation model, the Shockley–Read–Hall recombination (field enhancement) model, and the band-to-band tunneling model [4].

Secondly, for a test set (device and spatial parameters for 1,000 devices), the trained model predicts the initial solutions and these initial solutions are loaded. Finally, a numerical simulation is conducted directly at the target bias step, without any bias ramping procedure. If the simulation does not converge, a solution of the failed device is calculated by a conventional simulation with the bias ramping procedure. The LGBM model is retrained with that solution. This process made it possible to make highly accurate predictions for device with a wide range of parameters.

Figs. 4 and **5** show that our simulation flow is more efficient than the conventional bias ramping method in terms of the number of iterations required to obtain the target bias solution. The computational cost can be significantly reduced by avoiding unnecessary ramping steps. As a result, the target bias solutions of DRAM cells can be calculated within (at least) 13 times fewer Newton iterations.

CONCLUSION

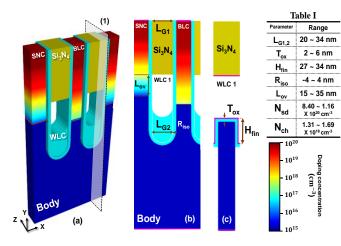
We have proposed the efficient simulation flow to obtain the target bias solutions of $6F^2$ DRAM cells with geometric fluctuation. The proposed simulation flow is highly efficient in analyzing the devices with these variations at a target bias. Compared with the conventional bias ramping procedure, the computational time can be significantly (at least 13 times) reduced.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) through the Korean Government under Grant NRF-2020M3H4A3081800.

REFERENCES

- S. Jeon et al., "Investigation on the local variation in BCAT process for DRAM technology", IEEE IRPS, (2017).
- [2] S. -C. Han et al., "Acceleration of Semiconductor Device Simulation with Approximate Solutions Predicted by Trained Neural Networks", IEEE Trans. Electron Devices, (2021)
- [3] G. Ke et al., "LightGBM: A highly efficient gradient boosting decision tree", in Proc. Adv. Neural Inf. Process. Syst., (2017)
- [4] J. H. Park et al., "Row Hammer Reduction Using a Buried Insulator in a Buried Channel Array Transistor", IEEE Trans. Electron Devices, (2022)



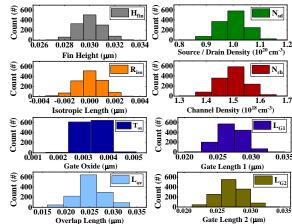


Fig. 1. (a) Schematics of the BCAT DRAM structure, (b) front side of structure, (c) view of a cross section cut by plane (1). Table I. Ranges of structure parameters.

Fig. 2. Distributions of 1300 device parameters ($L_{G1,2}$, L_{ov} , T_{ox} , H_{fin} , R_{iso} , N_{sd} , and N_{ch}).

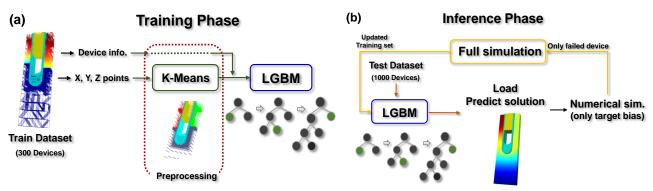
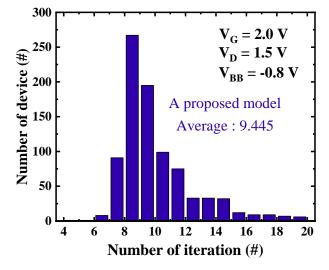


Fig. 3. Schematic for the entire process of ML-TCAD framework. (a) Training phase. The spatial parameters were preprocessed by K-means clustering, and high-accuracy model was bulited by adding cluster information to the input parameters. (b) Inference phase. The incremental training is used to make highly accurate predictions for device with a wide range of parameters.



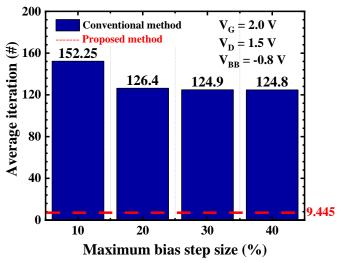


Fig.4. Distribution of the number of iterations for 1,000 devices, when the proposed method is applied at $V_G = 2.0$ V, $V_D = 1.5$ V, and $V_{BB} = -0.8$ V.

Fig. 5. Comparison of the average number of Newton iterations of the two methods at $V_G = 2.0 \text{ V}$, $V_D = 1.5 \text{ V}$, and $V_{BB} = -0.8 \text{ V}$. Our method converges within (at least) 13 times fewer iterations.