Simulation of Single-Electron Shuttling for Spin-Qubit Transport in a SiGe Quantum Bus

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Introduction

Spin qubits in gate-defined semiconductor quantum dots (QDs) are one of the major candidates for the realization of fault-tolerant universal quantum computers. Ongoing advances in the growth of SiGe heterostructures with isotopically purified ^{28}Si quantum wells have enabled exceptionally long coherence times. Moreover, the compatibility with industry standard fabrication technology opens up excellent prospects for scaling up SiGe-based quantum processors to very large numbers of qubits. Recently, small-scale devices have been demonstrated, which execute one- and two-qubit logic gates as well as initialization and read-out operations with high fidelity using all-electrical control.

The wiring and interconnection of large arrays of tunnel-coupled QDs, however, is a challenging problem as numerous control signals must be routed from external sources to every QD [1]. While control lines can be stacked in multiple layers, there are clear limitations in view of geometric constraints. A possible solution to this *fan-out problem* is partitioning of the qubit register into smaller QD arrays interconnected by coherent quantum links. Ref. [2] describes the design of such a scalable quantum bus, which allows to shuttle electrons using moving QDs along a one-dimensional channel in a *conveyor belt mode*, see Fig. 1. The quantum bus design provides sufficient space for QD wiring and classical on-chip control electronics.

Numerical Simulation

We present a framework for device-scale simulation of qubit shuttling in a SiGe quantum bus. Our goal is to assess the transfer fidelity of the electron and its spin state as it travels along the channel in the presence of material defects (*e.g.*, charged defects, interface inhomogeneity, etc.) and noise. The electrostatic potential of the control fields (clavier gates, screening gates, back gate), see Figs. 1–3, and the defect potential are computed by solving Poisson's equation using the Julia-package VoronoiFVM.jl [3]. The potentials are passed to WavePacket [4] for numerical simulation of the electron using either the time-dependent Schrödinger equation or a Lindblad-type quantum master equation. The latter allows to include phonon-assisted relaxation from excited orbital and valley states. We discuss optimization of the device geometry and give an outlook on optimal control of gate voltages for optimal steering of the qubit to minimize the effects of perturbations.

Acknowledgment

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References

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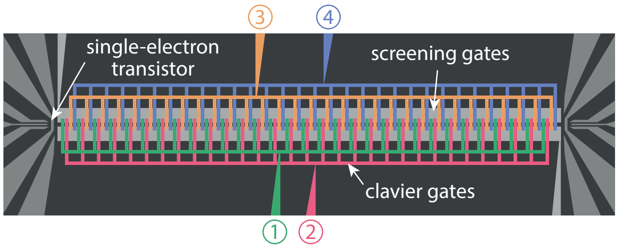

Fig. 1. Top view on the quantum bus, cf. [2]. Electrons are loaded and detected using single-electron transistors at both ends. By applying a sine-like pulse sequence on the clavier gate sets, a moving QD potential for qubit shuttling is formed.

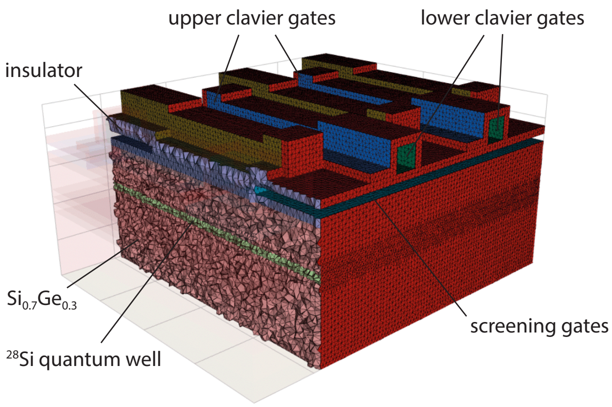

Fig. 2. Boundary conforming Delaunay mesh (generated with TetGen) for computation of the electrostatics problem using the finite volume method implemented in VoronoiFVM.jl [3].

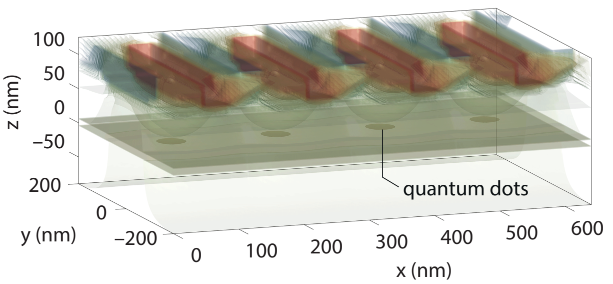

Fig. 3. Control potential generated by appropriate biasing of clavier gates and screening gates. A series of gate-defined quantum dots is formed in the center of the channel.

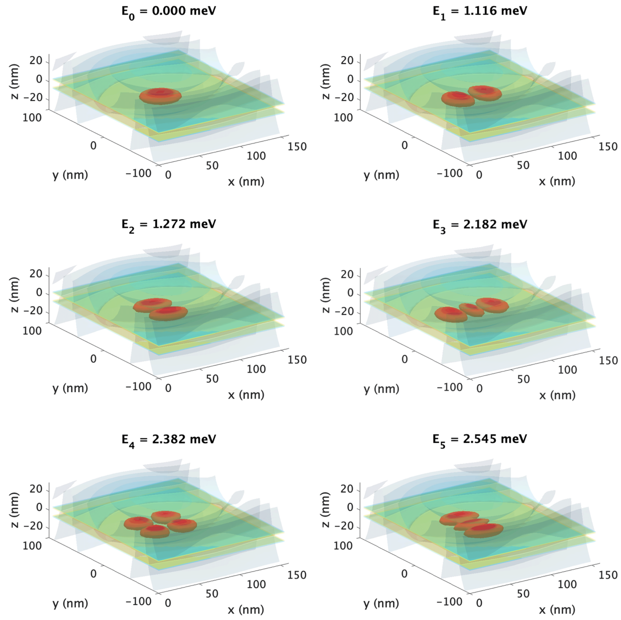

Fig. 4. Lowest energy bound states of an electron in a single periodic segment (four clavier gates) in a stationary frame computed using WavePacket [4]. The spectrum resembles that of a two-dimensional anisotropic harmonic oscillator.

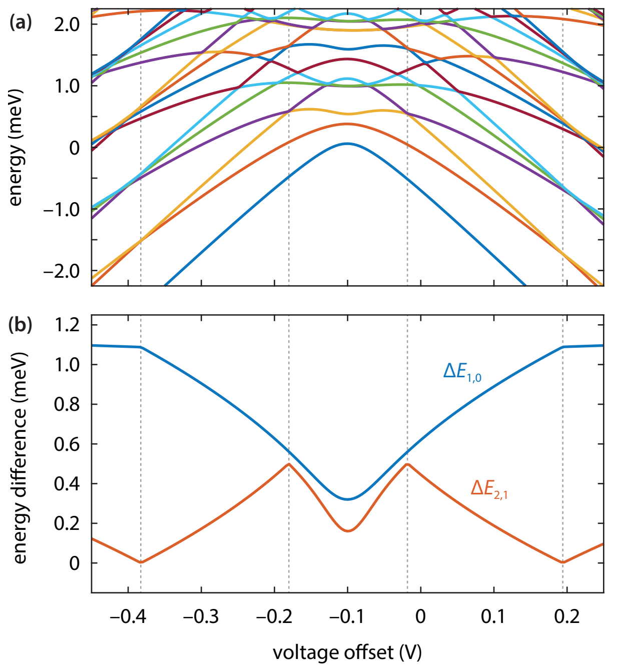

Fig. 5. (a) Bound state energies and (b) level separation as a function of the voltage amplitude offset between the lower and upper clavier gates. By tuning the voltage offset, the fundamental orbital splitting $\Delta E_{1,0}$ and the excited state degeneracy $\Delta E_{2,1}$ can be controlled.