Process Simulation in Micro- and Nano-Electronics

L. Filipovic[1]*, T. Reiter[1], X. Klemenschits[2,3], S. Leroch[1], R. Stella[1], O.Baumgartner[3], A. Hössinger[4]
[1]CDL for Multi-Scale Process Modeling of Semiconductor Devices and Sensors at the
[2]Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Vienna, Austria
[3]Global TCAD Solutions, Bösendorferstraße 1/1/12, 1010 Vienna, Austria
[4]Silvaco Europe Ltd., Compass Point, St Ives, Cambridgeshire, PE27 5JL, United Kingdom
*E-mail: filipovic@iue.tuwien.ac.at

The continued transistor miniaturization, the introduction of novel materials and geometries in complementary semiconductor-metal-oxide (CMOS) fabrication, and the ever-increasing complexity of the processes required for modern integrated circuits (ICs) must be supported by proper process- and device-technology computer aided design (TCAD) tools. Improvements in performance, power efficiency, and area density (PPA) from one technology node to the next nowadays involves substantial architectural and material innovations through TCAD-supported design-technology co-optimization (DTCO) [1], [2] (cf. Fig. 1).

Process simulation does not describe a single modeling approach and the complexities involved often span over many time and size scales, require the integration of several frameworks and data structures, and demand the application of models which range from highly physical to simplified geometric reconstructions [3]. Here, we describe some critical methodologies including applying different surface and volume descriptions in the same framework, merging physical and geometric (compact) models, and the multi-scale integration of atomistic molecular dynamics (MD) for process TCAD.

Process simulation can refer to topography simulations (e.g., surface etching and deposition) or volume processes (e.g., ion implantation, annealing, diffusion, oxidation), each requiring a unique modeling approach. Topography motion is often represented implicitly using the level set (LS) method, while volume processes require an explicit volume representation. We present the ViennaPS framework (cf. Fig. 2) which combines these approaches, allowing to simultaneously solve volume and surface problems. This allows to model, e.g., plasma impact damage during sputter etching [4] (cf. Fig. 3) and oxide redeposition during selective Si_3N_4 etching in 3D NAND structures [5].

For DTCO it is often necessary to provide quick process-aware structures, meaning that physical simulations are unfeasible. For this, we have pioneered the concept of process compact models, which are trained using combined measurements and physical simulations (cf. Fig. 4). The compact models can either be based on geometric equations whose inputs are functions of process parameters, or on process emulation through geometric advection, whereby the new surface is redrawn from each surface point, based on a known process-aware distribution [6]. The compact model approach has been applied to quantify the impact of fabrication conditions on the generation of air spacers at the 7 nm technology node and on their subsequent effect on the performance of a 5-stage ring oscillator (RO) [3]. The results (cf. Fig. 5) allow us to optimize the fabrication conditions towards improving PPA.

Finally, with the introduction of new materials, it has become increasingly important to study fabrication at the atomistic level, since experiments alone are too time- and cost-intensive. Therefore, a multi-scale link between atomistic MD and continuum TCAD modeling must be made. We are studying the formation of Al-doped 4H-SiC devices using this approach (cf. Fig. 6), whereby the atomistic analysis of the SiC film at different stages of the doping process (e.g., post ion implantation, post-annealing) must be analyzed. This allows to study the role of defects, interstitials, and vacancies on dopant activation and the subsequent fabrication steps.

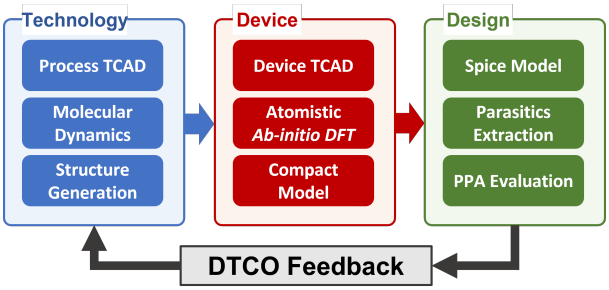

Fig. 1. Simplified DTCO flow for new designs, incorporating multi-scale process and device simulations as well as a feedback loop between circuit design and fabrication technology.

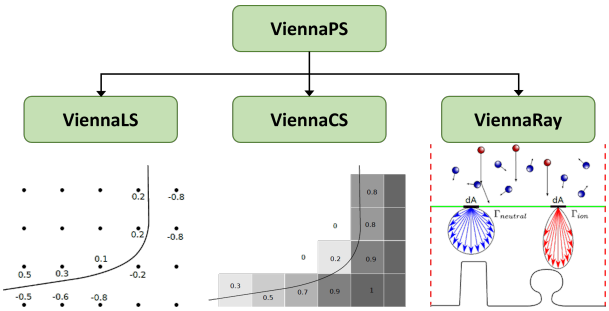

Fig. 2. Process simulation (PS) framework ViennaPS [7] including a level set (LS) surface definition, a cell set (CS) volume description, and a ray tracer for physical modeling.

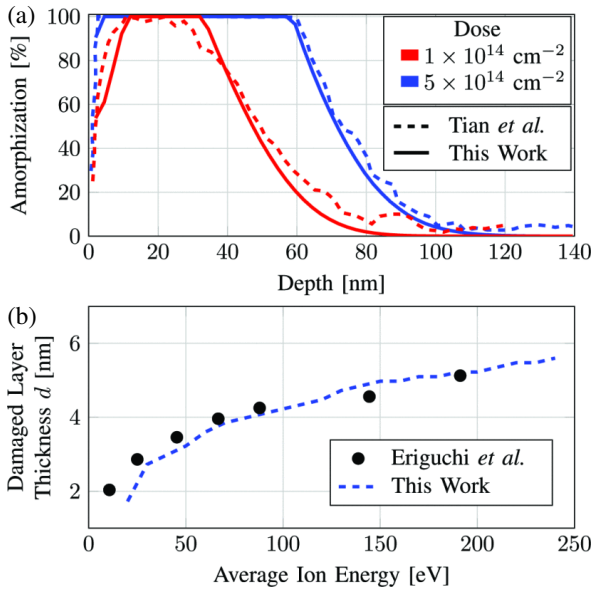

Fig. 3. (a) Comparison of the computed amorphization profile for high energy ions (50 keV) of an As implant process to the results obtained by Tian *et al.* [8]. (b) Impact of average ion energies on the thickness of the damaged (non-crystalline) layer compared to experimental data by Eriguchi *et al.* [9].

ACKNOWLEDGMENT

The financial support by the Austrian Federal Ministry for Digital and Economic Affairs, the National Foundation for Research, Technology and Development and the Christian Doppler Research Association is gratefully acknowledged. Support in-part by the Austrian Research Promotion Agency FFG Project 878662 PASTE-DTCO. Many thanks for contributions from J. Piso, J. Bobinac, and B. Bamer.

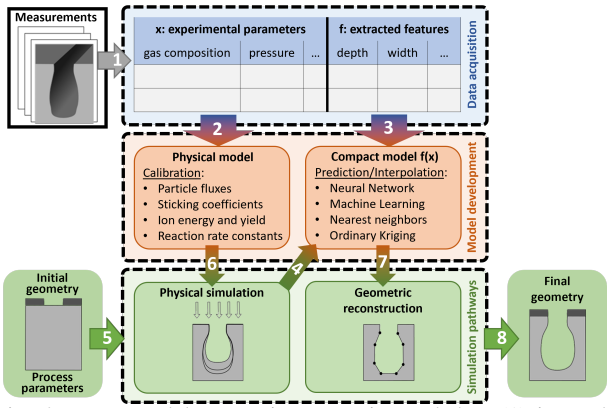

Fig. 4. For model generation, experimental data (1) is used to calibrate physical models (2), while a compact model is trained using experiments (3) and physical simulations (4). A simulation from initial conditions (5) can use a physical model (6) or a compact model (7) to obtain the final geometry (8).

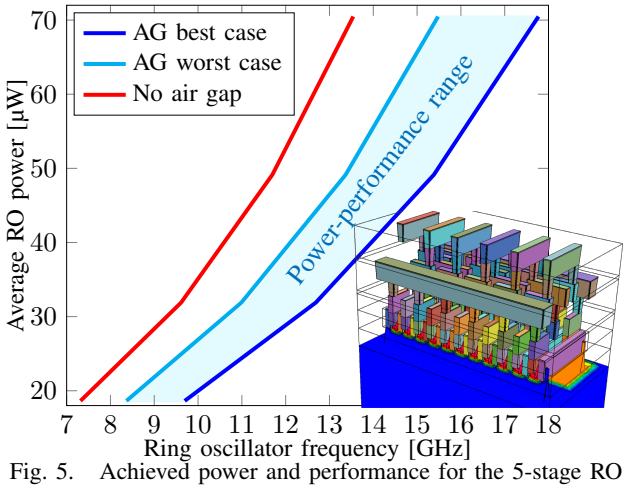

Fig. 5. Achieved power and performance for the 5-stage RO with no air gap (AG) and with an AG under the best and worst tested process conditions during spacer generation.

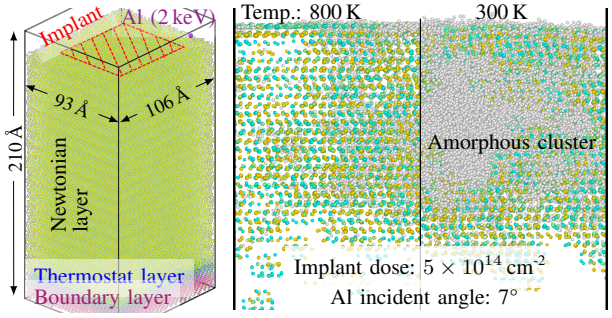

Fig. 6. MD setup of Al implantation in 4H-SiC (left) allows to study the resulting defects, vacancies, and interstitials (right).

REFERENCES

[1] Z. Zhang *et al.*, in SNW, 2pp, 2019.
[2] L. Yuan, in *TSMC Blog*, 2022.
[3] L. Filipovic *et al.*, *SSE* **199**, No. 108527, 2023.
[4] T. Reiter *et al.*, in *IEEE IIRW*, 5 pp, 2022.
[5] Z. Zhou *et al.*, *JIEC* **119**, pp. 218–225, 2023.
[6] X. Klemenschits *et al.*, *CMAME* **386**, No. 114196, 2021.
[7] ViennaPS-1.2.0. https://github.com/ViennaTools.
[8] S. Tian *et al.*, *IEEE TED* **45**(6), pp. 1226–1238, 1998.
[9] K. Eriguchi *et al.*, *JJAP* **49**, No. 056203, 2010.