Modeling Self-Heating Effects in 28 nm Technology Node Fully-Depleted SOI Devices

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Recently, excellent characteristics at 4.2K were demonstrated for Fully-Depleted (FD) SOI technologies. These electrical characteristics represent a great opportunity to use advanced CMOS in low-temperature environments such as space applications. Also, due to recent efforts to bring down quantum computing into mainstream technology, cryogenic control electronics for quantum computing is becoming of significant interest for low-temperature MOSFET operation.

In FDSOI devices the heat generated at the drain side is impeded by the low thermal conductivities of the buried oxide (BOX) and the thin Si layer constituting the channel (due to phonon boundary scattering). Self-heating effects (SHE) lead to a significant increase in the channel temperature when the device is in its on-state. The channel temperature increase can severely affect the device performance by reducing the carrier mobility. Extensive studies, both experimental [1] and theoretical [2], are already conducted and published for room temperature device operation. Also, experimental studies were performed recently to understand SHE in FDSOI devices at cryogenic temperatures [3]. Hence, there is a need for simulation software able to explain existing experimental data and make reliable predictions for FDSOI devices with different channel lengths, silicon film and BOX thickness at various temperatures.

For that purpose, we developed a thermal device simulator for modeling SHE in FDSOI devices at temperatures down to 78K. Details about the theoretical model of our electro-thermal device solver can be found in Ref. [2]. Briefly, we solve the electron Boltzmann Transport Equation (BTE) using the Monte Carlo method self-consistently with the energy balance equations for both the acoustic and the optical phonons. We account for the partial ionization of the dopants and the temperature and the thickness dependence of the thermal conductivity.

The device structure of interest (28nm technology node with 30 nm physical channel length n-FDSOI device with 7 nm silicon film thickness, 1.2 nm effective gate oxide and 25 nm thickness of the BOX) is schematically shown in Fig. 1. Simulated transfer characteristics (Fig. 2) are first compared with available experimental data at T=300K [3]. Excellent agreement is observed between the experimental and simulated data in both sub-threshold and linear regions of operation of the device. In Fig. 3, we show the simulated transfer characteristics at T=78K, 150K and 300K. We observe that, at lower temperatures, the threshold voltage slightly increases due to the partial ionization of the dopants, in agreement with the experimental findings [3]. The lattice temperature profile at ambient temperature T=300K, and for Vgs=0.6V and Vds=0.9V, is shown in Fig. 4. In these simulations it is assumed that the source and drain contacts are perfect absorbers of heat. In Fig. 5, we show a comparison of the simulated and the experimental excess temperature in the channel for various input powers and for ambient temperatures T=78K, 150K and 300K. Experimentally, self-heating was obtained using the well-known gate resistance thermometry technique [1]. In this method, the thin gate dielectric layer allows one to assume that the temperature of the channel and that of the gate electrode are almost the same. Even though simulated channel temperatures are slightly higher at lower input power than the experimentally extracted values, the slope of the two curves, which gives the thermal resistance, is very similar. The discrepancy between the experimental

and the simulated data is attributed to the uncertainties in the experimental device dimensions and the simplified zero heat flux boundary condition for the lattice temperature on the gate electrode.

In summary, this work intends to fill the gap in obtaining relevant simulation data concerning self-heating in advanced FDSOI transistors at various temperatures.

REFERENCES

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[2] K. Raleva, D. Vasileska, S. M. Goodnick and M. Nedjalkov, *Modeling Thermal Effects in Nanodevices,* IEEE Trans. Electron Devices **55**, no. 6, pp. 1306-1316 (2008).

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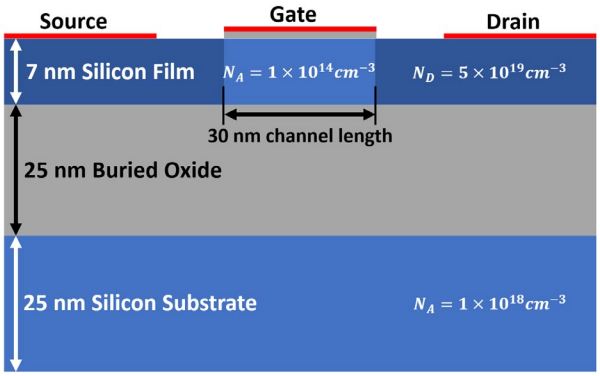

Fig. **1**. FDSOI device structure being considered in this study.

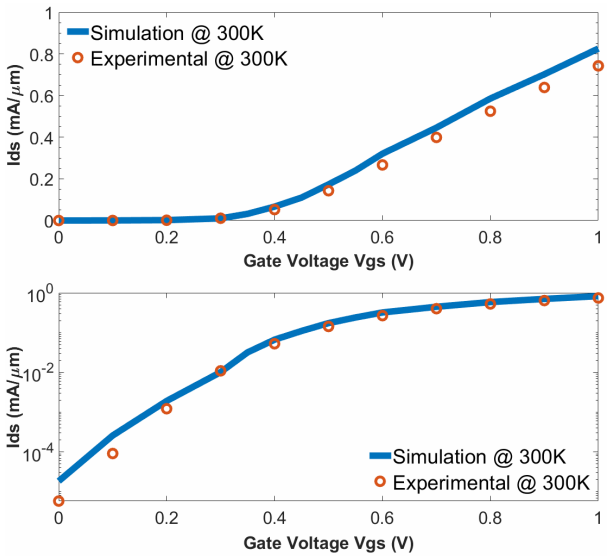

Fig. 2. Simulated transfer characteristics compared with available experimental data from Ref. [3] at T=300K. The applied drain voltage is Vds=0.9V.

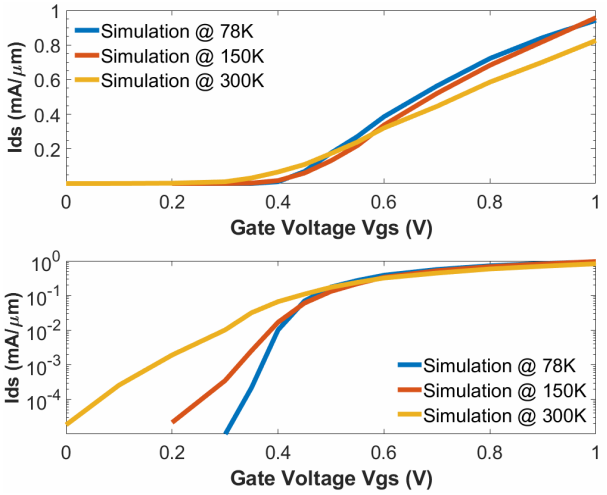

Fig. 3. Simulated transfer characteristics at 78K, 150K and 300K. The applied drain voltage is Vds=0.9V.

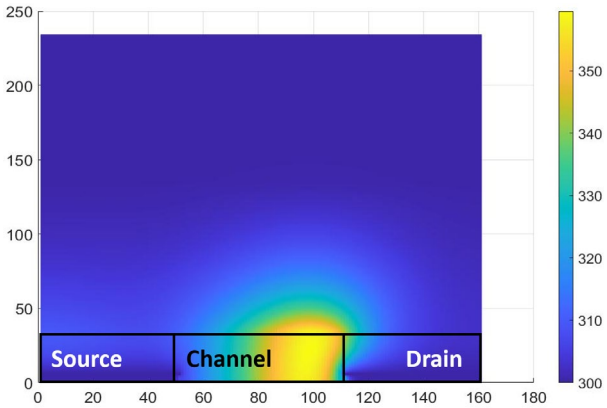

Fig. 4. Lattice temperature profile at ambient temperature T=300K for Vgs=0.6V and Vds=0.9V. We used boundary conditions with fixed temperature T=300K at source and drain contacts, and boundary condition with zero heat flux at the gate contact.

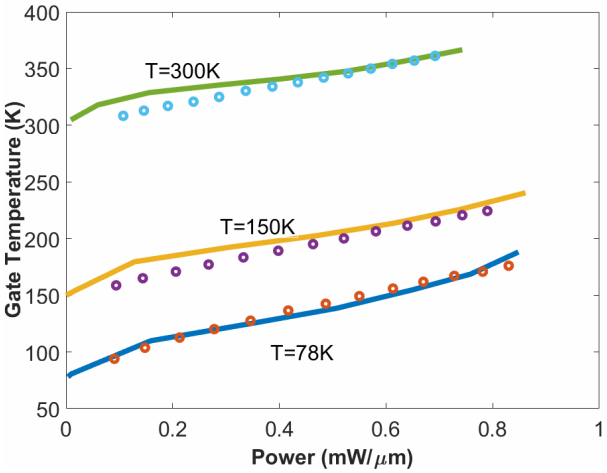

Fig. 5. Comparison of simulated (solid lines) and experimental (open circles) temperature under the gate for various input powers at T=78K, 150K and 300K.