Extending the small-signal modeling of GFETs to ambipolarity regime

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1. Abstract

Analog/RF circuit design with Graphene field-effect transistor (GFET) technology, continually grows due to exceptional extrinsic maximum oscillation (f_{max}) and cut-off frequencies (f_t), recorded for the specific device [1]. We have recently proposed an efficient small-signal GFET parameter extraction procedure, targeting on Quasi-Static regime [2]. Our methodology is based on a charge-based model [3] which ensures charge conservation in the intrinsic device. Both the bias- and frequency- dependence of the total of small-signal parameters have been accurately validated with experiments from a short-channel RF CVD GFET [4], up to 18 GHz for a unipolar (p-type) region of operation. In the present study, the complete ambipolar small-signal response of short-channel GFETs [5], [6] is demonstrated, including the charge neutrality point or Dirac voltage (V_{Dirac}), with remarkable agreement between models and experiments. The bias region around V_{Dirac} is of outmost significance in certain applications of ambipolar devices such as GFET, as it can ensure multifunctionality [7].

2. DUT and Measurement Setup

High frequency measurements are conducted in the present work for two short-channel back-gated RF CVD GFETs with gate width W=12x2 μm (number of gate fingers:2) and gate length L=200 nm, 300 nm, respectively [5], [6]. They are fabricated by the same group as the device studied in [2], but from a different technology process and thus, they present dissimilar characteristics such as higher contact resistance R_C. They have also been examined in terms of thermal noise experimental characterization and modelling at 1 GHz [6]. In the current work, S(Y) parameters are measured and small-signal parameters are investigated after appropriate de-embedding and R_C-gate resistance R_G elimination procedures [8], [2], [6] up to or even above f_t. Details on the devices' schematics and measurement setups can be found in [5], [6].

3. Results and Discussions

The small-signal sub-circuit model employed in this study, has been presented elsewhere [2 (Fig. 1a)]. As a first step of this work, IV model parameters are extracted, similarly as in [2], for both devices under test (DUT), and presented in Table I; μ is the carrier mobility, C_{back} the back-gate capacitance, Δ the inhomogeneity of the electrostatic potential, related to the residual charge, u_{sat} the saturation velocity while the rest of the parameters (V_{Dirac}, R_C, R_G) have already been defined. Magnitude and phase of all the measured S_{DEV} parameters for both DUT at a drain voltage V_{DS}=0.5 V, are presented vs. V_{GS} at 1 GHz (cf. Fig. 1) and vs. frequency at two V_{GS} values (cf. Fig. 2), near and exactly at V_{Dirac} point, respectively (V_{GS}=0.3, 0.5 V for L=200nm, V_{GS}=0.4, 0.6 V for L=300 nm). The consistency of the extracted models is also highlighted from p- to n-type region including V_{Dirac}, while observed disparities at higher frequencies (cf. Fig. 2) arise from non-quasi-static (NQS) effects due to low f_t of the devices [9]. The recorded model agreement with experiments at V_{Dirac} is prerequisite for reliable circuit design in RF GFET applications such as phase/frequency configurable amplifiers, frequency doublers, in-phase power and inverting amplifiers, which operate near or at the specific neutrality point [7]. Inconsistencies observed in the magnitude of S_{21DEV} at n-type region are due to measurement asymmetries between hole and electron branches, and can be accounted by considering distinct models for the two conductance regimes [9].

After rigorous removal of $R_{C,G}$ contributions, intrinsic small-signal parameters of the DUT, such as capacitances C_{GG}, C_{GD}, C_{DG}, cut-off frequency f_{tINT}, and small-signal current gain $|h_{21INT}|$, can be extracted [2]. Other significant extrinsic figures of merit, such as $f_{tEX,}$ $|h_{21EXT}|$, and unilateral power gain U, can also be derived directly from de-embedded $S(Y)_{DEV}$ measurements [2]. C_{GG}, C_{GD}, C_{DG} (cf. Fig. 3), $f_{tINT,EX}$, f_{max} (cf. Fig. 4), and $|h_{21INT,EX}|$, U (cf. Fig. 5), are depicted for both DUT at 1 GHz for V_{DS}=0.5 V, vs. V_{GS} where the models capture precisely the experiments, especially around V_{Dirac}, which is of special interest in the current analysis. Intrinsic capacitances present a minimum at V_{Dirac} and afterwards, increase towards higher carrier densities. Besides, $f_{tINT,EX}$, $f_{max,}$ $|h_{21INT,EX}|$, U parameters follow an M-shape trend with a minimum at V_{Dirac} while, they are significantly reduced (for the L=300 nm device) in comparison with a GFET with same L but much lower R_C in [2]. The latter highlights the negative effect of R_C on small-signal parameters and thus, justifies the aforementioned NQS effects below 5 GHz (cf. Fig. 2).

Table 1. IV extracted parameters

Parameter	Units	L=200 nm	L=300 nm
μ	$cm^2/(V{\cdot}s)$	200	170
u_{sat}	m/s	$7x10^5$	$7x10^5$
C_{back}	$\mu F/cm^2$	1.87	1.87
V_{Dirac}	V	0.5	0.6
R_c	Ω	130	180
R_G	Ω	18	12
Δ	meV	150	165

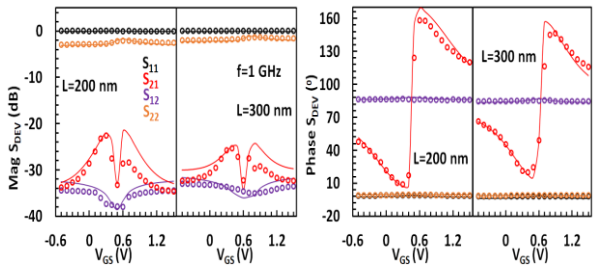

Fig. 1. Magnitude (left plot) and phase (right plot) of de-embedded S-parameters (S_{DEV}) for two GFETs with gate width W=24 µm and length L=200 nm (left subplots), L=300 nm (right subplots) vs. gate voltage V_{GS} for operation frequency f=1 GHz at a drain voltage V_{DS}=0.5 V. Markers: measurements, lines: model.

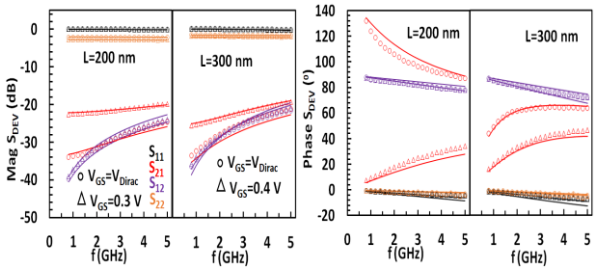

Fig. 2. Magnitude (left plot) and phase (right plot) of de-embedded S_{DEV} for two GFETs with W=24 µm and L=200 nm (left subplots), L=300 nm (right subplots) vs. f for two V_{GS} values; near and at Dirac Voltage at V_{DS}=0.5 V. Markers: measurements, lines: model.

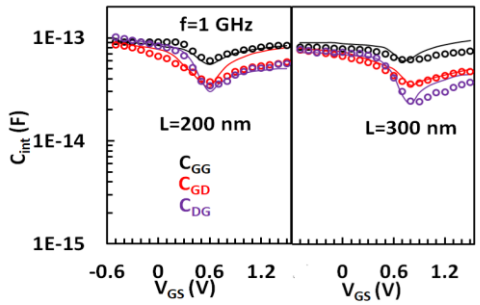

Fig. 3. Intrinsic capacitances C_{GG}, C_{GD}, C_{DG}, respectively for two GFETs with W=24 µm and L=200 nm (left subplot), L=300 nm (right subplot) vs. V_{GS} for f=1 GHz at V_{DS}=0.5 V. Markers: measurements, lines: model.

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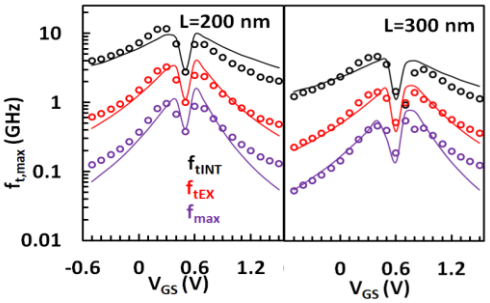

Fig. 4. Intrinsic, extrinsic cut-off and extrinsic maximum oscillation frequencies f_{tINT}, f_{tEXT}, f_{max}, respectively for two GFETs with W=24 µm and L=200 nm (left subplot), L=300 nm (right subplot) vs. V_{GS} at V_{DS}=0.5 V. Markers: measurements, lines: model.

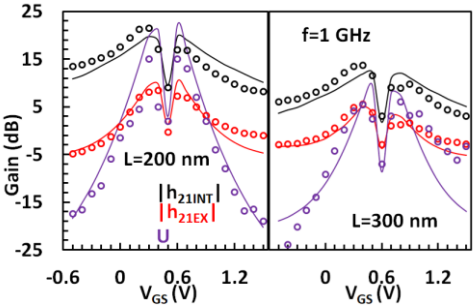

Fig. 5. Intrinsic, extrinsic small-signal current gain and unilateral power gain $|h_{21INT}|$, $|h_{21EX}|$, U, respectively for two GFETs with W=24 µm and L=200 nm (left subplot), L=300 nm (right subplot) vs. V_{GS} for f=1 GHz at V_{DS}=0.5 V. Markers: measurements, lines: model.

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