Schottky barriers in one-dimensional field-effect transistors: a model-based characterization

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INTRODUCTION

The characterization of the the metal-channel interfaces is of outmost importance for one-dimensional (1D) Schottky field-effect transistor (FET) technologies. The dimensionality of the channel impacts on the injection mechanisms at the Schottky contacts and hence, on the interface characteristics such as the potential barrier height [1]-[4]. The latter device parameter is proven to be underestimated in 1D channel transistors if conventional extraction techniques, e.g., the three-dimensional (3D) activation energy method (AEM), are used. Such approaches rely on the physics of 2D contacts and 3D channels which differ from the phenomena at 3D-metal-1D-channel interfaces [2]-[4]. In this work, a parameter extraction methodology for potential barrier heights in 1D FETs within the context of 1D Landauer-Büttiker transport model is reviewed. The model-based characterization method is applied to fabricated and simulated carbon nanotube (CNT) FETs and nanowire (NW) FETs with single- and multiple-channels (cf. Fig. 1). Studies on the impact of a displaced gate as well as of channel Schottky points on the extracted values are carried out with numerical device simulations.

SCHOTTKY BARRIER HEIGHT EXTRACTION

The thermionic drain current I_D of a 1D FET, corresponding to operation at the subthreshold regime, can be approximated as [1], [5]

$$I_\mathrm{D} \approx \Upsilon \exp\left[\frac{n_\mathrm{g}}{V_\mathrm{t}}\left(V_\mathrm{GS}-V_\mathrm{FB}\right)+\frac{n_\mathrm{d}}{V_\mathrm{t}}V_\mathrm{DS}-\frac{\Phi_\mathrm{BH,eff}}{V_\mathrm{t}}\right], \tag{1}$$

where $\Upsilon = (4q^2/h)\,V_\mathrm{t}\mathcal{T}_\mathrm{th}$ with q as the electronic charge, h the Planck constant, $V_\mathrm{t} = k_\mathrm{B}T/q$ the thermal voltage with k_B as the Boltzmann constant and T the absolute temperature, $\mathcal{T}_\mathrm{th}$ is the thermionic transmission probability, n_g and n_d are gate and drain coupling coefficients [5], respectively, V_GS and V_DS are the gate-to-source and drain-to-source voltage, $\Phi_\mathrm{BH,eff}$ is an effective potential barrier height at which pure thermionic injection ocurrs in the 1D device and V_FB is the flatband voltage (cf. Fig. 2). Conditions for obtaining Eq. (1) have been explained in detail in [2] and an adapted form for considering multi-1D-channels has been presented in [4]. For quasiballistic 1D devices $\mathcal{T}_\mathrm{th} \approx 1$ at low-fields and hence, Eq. (1) can be rearranged such as [2], [4]

$$\Phi_\mathrm{BH,eff} = n_\mathrm{q}\left(V_\mathrm{GS}-V_\mathrm{FB}\right)+\Phi_\mathrm{SB,eff} \tag{2}$$

where $\Phi_\mathrm{SB,eff} = n_\mathrm{d}V_\mathrm{DS} - (k_\mathrm{B}/q)\alpha$ is an effective Schottky barrier height and α is the slope of an Arrhenius plot ($\ln(I_\mathrm{D}T^{-1})$ vs. T^{-1}). $\Phi_\mathrm{SB,eff}$ is the parameter useful to evaluate the quality of the contacts and it is obtained from Eq. (2) at $V_\mathrm{DS} = 0$ and $V_\mathrm{GS} = V_\mathrm{FB}$. The latter point is obtained at the onset of tunneling phenomena corresponding to a change of slope in a $\Phi_\mathrm{BH,eff}$ vs. V_GS plot. The 1D Landauer-Büttiker extraction method (1D LBM) shown here is visualized in Fig. 3 where it has been applied to experimental data of a CNTFET and a NWFET with multiple 1D channels, as reported elsewhere [4].

NUMERICAL DEVICE SIMULATIONS

Simulations of BG CNTFETs have been performed with an experimentally verified in-house numerical CNTFET simulator using a self-consistent solution of a transport equation and the Poisson equation, presented elsewhere [6], [7] in order to *(i)* explore the limits of the methodology (cf. Fig. 4), *(ii)* propose a test structure to ease the extraction (cf. Fig. 5) and *(iii)* study specific imperfections affecting the extracted values, e.g., Schottky points within the channel (cf. Fig. 6).

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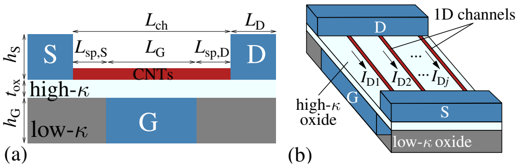

Fig. 1. Schematic (a) cross-section and (b) device structure of a buried-gate CNTFET simulated in this work [2]-[4].

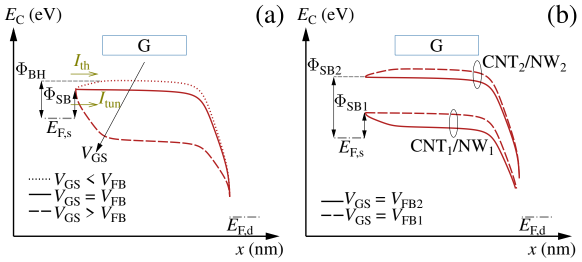

Fig. 2. Conduction band diagrams of a 1D-FET with (a) single-1D-channel and (b) multi-1D-channels at different V_{GS} [4].

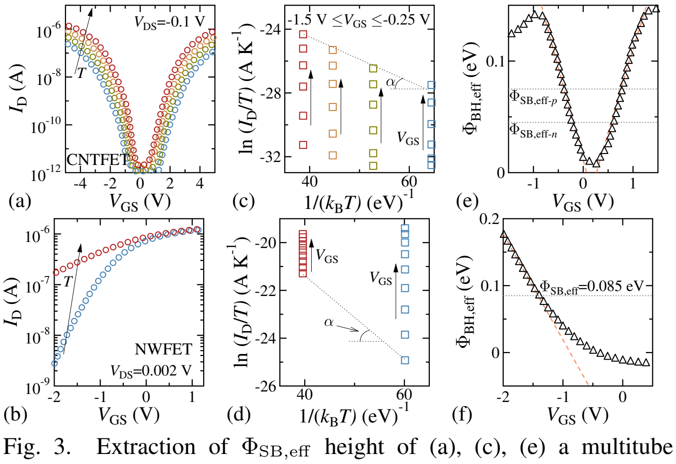

Fig. 3. Extraction of $\Phi_{SB,eff}$ height of (a), (c), (e) a multitube CNTFET and (b), (d), (f) a multiwire NWFET. Further details on experimental data, plots and related discussions are provided in [4].

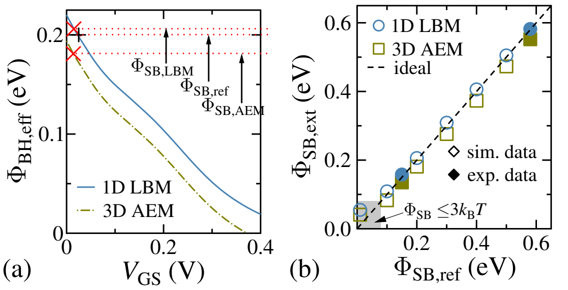

Fig. 4. Comparison between 3D AEM and 1D LBM using simulated BG CNTFETs with (a) 0.2 eV and (b) various values of Schottky barrier height. 1D LBM extracts a value close to the reference value set in simulations. Gray zone in (b) shows that both methods overestimate the value below ∼ 0.07 eV. Further details in [2].

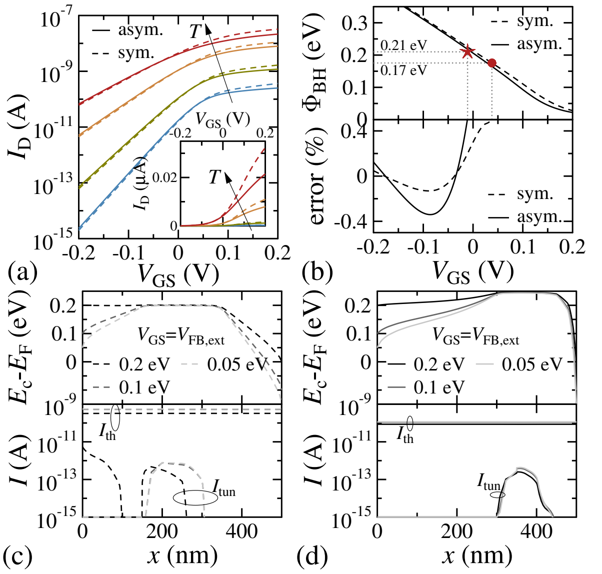

Fig. 5. Simulated symmetric and asymmetric multi-channel BG MT CNTFETs data. (a) Transfer characteristics at V_{DS}=0.2 V and different T. (b) $\Phi_{SB,eff}$ extraction from the barrier height potential plot over V_{GS} (top) and relative error related to a linear extrapolation of pure thermionic transport (bottom). Conduction band diagrams (top) and thermionic and tunneling currents along the channel (bottom) of the (c) symmetric and (d) asymmetric CNTFETs. Details in [4].

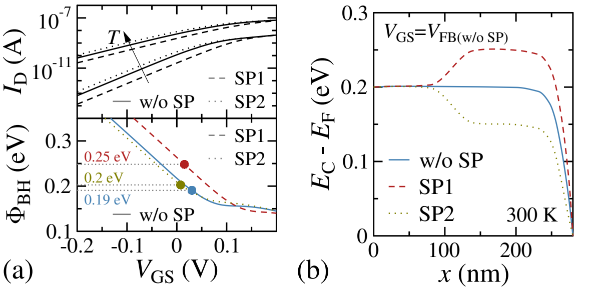

Fig. 6. Simulation results of multi-channel BG CNTFETs with and without different Schottky points. (a) Top: transfer characteristics (300 K and 500 K) at $V_{DS} = 0.2$ V; bottom: potential barrier height versus V_{GS} obtained with 1D LBM. (b) Conduction bands at the V_{FB} of the device without SP. Further details in [4].