Memristors with thousands of conductance levels for analog computing

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Abstract:

The analog data deluge issue nowadays call for multipurpose analog computing platforms with great reconfigurability and efficiency, namely, field-programmable analog arrays (FPAAs).[1] FPAAs as the analog counterpart of field-programmable digital arrays (FPGAs) open opportunities for fast prototyping analog designs as well as efficient analog signal processing and neuromorphic computing. Memristors may be the ideal building blocks for FPAAs if they are truly analog with many conductance levels, not just for lab-made devices, but more importantly, devices fabricated in foundries. We have recently demonstrated 2048 conductance levels, a record among all types of memories, achieved with memristors in fully integrated chips with 256 × 256 memristor arrays monolithically integrated on CMOS circuits in a standard foundry.[2] We have unearthed the underlying physics that previously limited the number of distinguishable conductance levels in memristors and developed electrical operation protocols to circumvent such limitations. These results reveal insights into the fundamental understanding of the microscopic picture of memristive switching and provide approaches to enable high-precision memristors for various applications.

Reference:

1 Li, Y., Song, W., Wang, Z., Jiang, H., Yan, P., Lin, P., Li, C., Rao, M., Barnell, M., Wu, Q., Ganguli, S., Roy, A.K., Xia, Q., and Yang, J.J.: 'Memristive Field-Programmable Analog Arrays for Analog Computing', Advanced Materials, 2022, pp. 2206648

2 Rao, M., Tang, H., Wu, J.-B., Song, W., Zhang, M., Yin, W., Zhuo, Y., Kiani, F., Chen, B., Jiang, X., Liu, H., Chen, H.-Y., Midya, R., Ye, F., Jiang, H., Wang, Z., Wu, M., Hu, M., Wang, H., Xia, Q., Ge, N., Li, J., and Yang, J.J.: 'Thousands of conductance levels in memristors integrated on CMOS', Nature, 2023, 615

J. Joshua Yang is a professor of the Department of Electrical and Computer Engineering at the University of Southern California. He was a professor of the ECE department at the University of Massachusetts Amherst between 2015 and 2020. He spent about 8 years at HP Labs between 2007 and 2015, leading the emerging devices team for memory and computing. His current research interest is Post-CMOS hardware for neuromorphic computing, machine learning and artificial intelligence, where he published several pioneering papers and holds 120 granted and about 60 pending US Patents. He is the Founding Chair of the IEEE Neuromorphic Computing Technical Committee, a recipient of the Powell Faculty Research Award and a recipient of UMass distinguished faculty lecturer and UMass Chancellor's Medal, the highest honor of UMass. He serves on the Advisory Boards of a number of prime international journals and conferences, including serving as an associate editor of *Science Advances*. Dr. Yang is a Clarivate™ Highly Cited Researcher in the field of Cross-Field and the Top Best Scientists in the Research.com list in the Electronics and Electrical Engineering category for 2022. He was elected to the IEEE Fellow and the National Academy of Inventors (NAI) Fellow for his contributions to resistive switching materials and devices for nonvolatile memory and neuromorphic computing.